SPERRY UNIVAC
1100/40 Systems

Hardware

System Description

SPERRY UNIVAC
COMPUTER SYSTEMS

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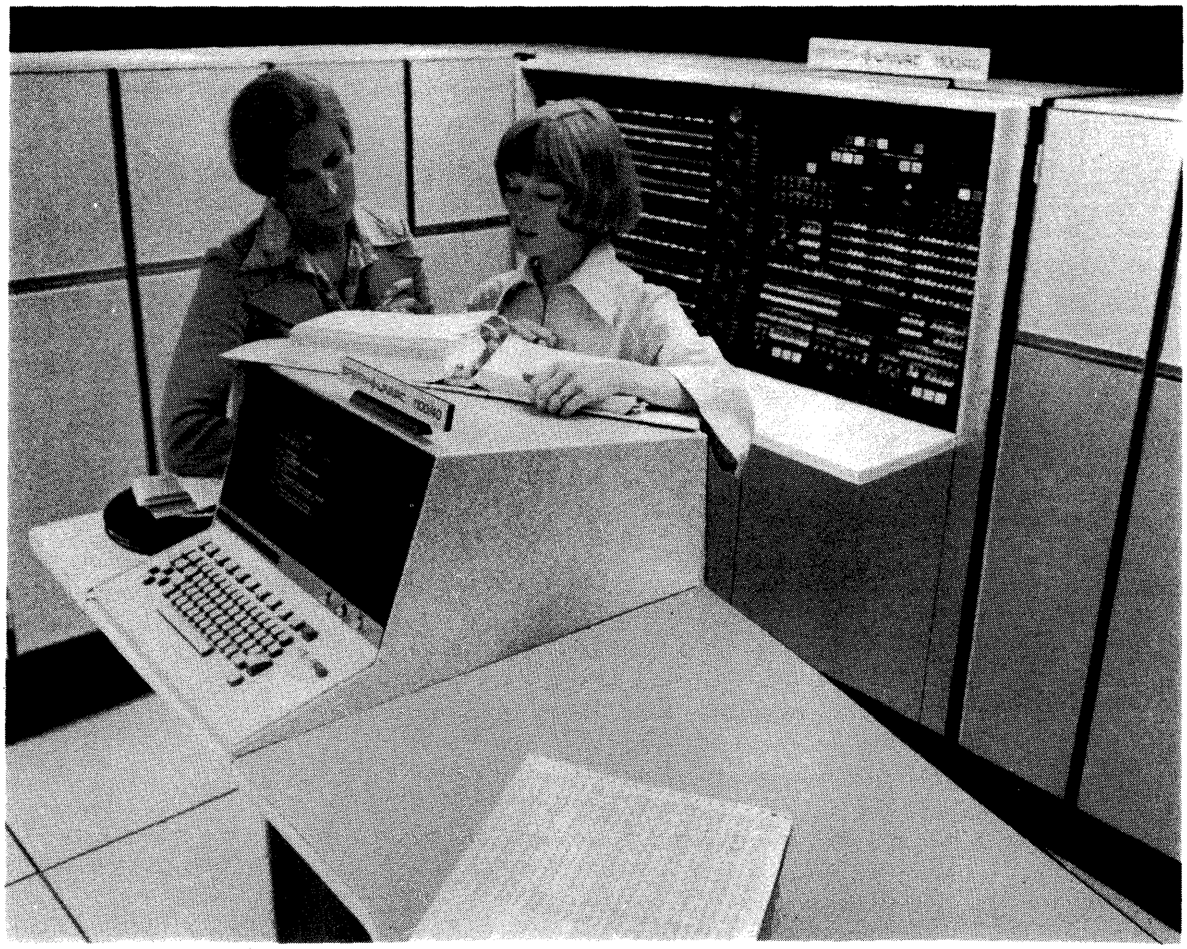


Figure 1–1. SPERRY UNIVAC 1100/40 System

The SPERRY UNIVAC 1100/40 Systems (see Figure 1–1) are a logical extension to the proven SPERRY UNIVAC 1100 Series Systems. Designed to enhance the efficiency of the SPERRY UNIVAC 1100 Series, the 1100/40 Systems offer dependable and highly effective processing in real time, demand, and batch modes, and excels in multiprocessing time-sharing applications.

Although the 1100 Series Systems may differ in hardware design, software compatibility is maintained. All components of the 1100/40 Systems (command/arithmetic units, input/output access units, storage units, and peripherals) are controlled by a SPERRY UNIVAC 1100 Series-operating system. Industry standard language processors and application software are provided. The uniqueness and flexible design of the 1100/40 Systems offer the user a variety of custom-tailored systems.

2. SYSTEM DESCRIPTION

2.1. GENERAL

The SPERRY UNIVAC 1100/40 Systems are a series of general purpose, high performance systems incorporating the latest advances in computer design, system organization, and programming technology. The various components of the 1100/40 Systems are designed as separate logical units providing maximum functional modularity. The multiprocessing capabilities are an integral part of the system; the command/arithmetic units can perform numerous tasks simultaneously under control of a common executive system. The flexible modular structure enables a user to tailor a system to his individual requirements. Principle features of the 1100/40 Systems are:

- common resource systems organization;
- multiple command/arithmetic units (CAUs) and input/output access units (IOAUs);
- independent input/output access units (IOAUs);
- two levels of directly addressable storage, multi-banking capabilities;
- large modular semiconductor primary storage (524K words maximum);
- large modular semiconductor extended storage (1048K words maximum);
- wide choice of high performance auxiliary storage and peripheral subsystems;
- independent, simultaneous communications processing;
- redundancy among system components;
- system partitioning capability;
- dynamic adjustment to a mix of batch, demand, and real time modes;
- extensive software library and language processors;
- character manipulating instructions;
- partial-word, double-word, and full-word addressability;
- storage protection;
- program address relocation; and
- a continuously evolving yet continuously compatible operating system.

2.2. SYSTEM COMPONENTS

Each component in the 1100/40 System is functionally independent and may have the following properties:

- Two or more access paths.
- Access conflicts resolved by priority logic.
- Continued system operation if any redundant component fails.
- Components can be logically removed for servicing without disabling the entire system.

The 1100/40 System consists of eight types of components:

- Command/Arithmetic Units
- Input/Output Access Units
- System Console
- System Partitioning Unit
- Primary Storage
- Extended Storage
- Maintenance Controller
- Auxiliary Storage and Peripheral Subsystems

2.2.1. Command/Arithmetic Unit (CAU)

The basic 1100/41 System configuration includes one command/arithmetic unit (CAU) and one input/output access unit. All control and arithmetic functions are executed by the CAU. The CAU is a multitask instruction-stacking device capable of controlling up to four instructions at various stages of execution. A CAU can interface with up to four primary storage units by means of both an instruction path and an operand path. Dual data paths connect the CAU with extended storage through a maximum of eight SPERRY UNIVAC Multiple Access Interface (MAI) units. The data paths to primary and extended storage have overlapping and interleaving capabilities. In a multiprocessor system the user can specify and can change which units are to be used, thereby permitting a system to be logically divided into two or three independent smaller systems, or removing individual units for maintenance without affecting the total system. Interrupt signals may be sent or received on one of the three interprocessor lines.

Additional features of each CAU are:

- capability of executing up to 1.8 million instructions per second;
- 300-nanosecond effective basic instruction time;
- four-deep instruction stack;

- 112-word general register stack (GRS); and

- character manipulation by means of partial word and byte-oriented instructions.

2.2.2. Input/Output Access Unit (IOAU)

The basic 1100/41 System configuration includes one input/output access unit (IOAU). The IOAU controls all transfers of data between the peripheral devices and primary and extended storage. Transfers are initiated by a CAU under program control. The IOAU includes independent data transfer paths to primary storage and to extended storage.

The IOAU consists of two sections: a control section and a section containing from 8 to 24 input/output channels. I/O data transfers may occur simultaneously with the execution of programs in the CAU.

The control section includes all logic associated with the transfer of function, data, and status words between primary or extended storage and the subsystems. It also services I/O requests from either one or both of the CAUs (in a multiprocessor system) and routes interrupts to one of the two command/arithmetic units. Interrupt routing may be specified by program.

Some outstanding features of an IOAU are:

- aggregate transfer rate of 4 million 36-bit words (24 million characters) per second;

- externally specified index (ESI) and internally specified index (ISI) transfer modes on any channel;

- data chaining;

- interrupt tabling;

- storage-to-storage transfers; and

- parity generation/checking capability on all ISI channels.

2.2.3. System Console

The system console provides the means for communication with the executive system. The basic console consists of the following major components:

- The CRT/keyboard consists of a UNISCOPE 100 Display Terminal. The display format is 16 lines with 64 characters per line. The seven-bit ASCII character set, consisting of 95 characters plus the space, is used. The keyboard provides all of the operator controls required for generating data and initiating transfers.

- The incremental printer operates at 30 characters per second and provides a hard copy of console messages. (One additional incremental printer may be connected to a console.)

- Interface for remote console operation by means of the Total Remote Assistance CEnter (TRACE) computer system. Sperry Univac customer engineers have the capability of analyzing system problems remote from the site.

- The fault indicator, located on the incremental printer, provides the operator with a visual indication of a fault condition in a major system component. The actual component and nature of the fault may then be determined from indicators on the maintenance panel.

2.2.4. System Partitioning Unit (SPU)

The system partitioning unit (SPU), when included in the 1100/40 System, permits offline maintenance of units, enables the operator to logically partition the system into two or three independent systems, and initiates a recovery sequence in the event of failure. The SPU performs six functions, five under operator control and one under software control. With the SPU, the operator can:

- partition the total system into two or three smaller systems;
- isolate units and take them offline for maintenance without disrupting the rest of the system;
- function as a system monitor by observing the status of the various major components;
- perform initial load into the primary system;
- allow automatic recovery procedures if an interrupt is not received.

Under software control, the SPU presents status information to the IOAU(s).

When all optional features are included, the SPU is able to interface with:

- four command/arithmetic units;
- four input/output access units;
- 524K words of primary storage;
- eight multiple access interface (MAI) units (1048K words of extended storage); and
- 48 multi-access subsystems.

2.2.5. Primary Storage

The first level of directly addressable main storage in the 1100/40 Systems is primary storage. Primary storage consists of high speed, nondestructive readout (NDRO), semiconductor storage units with nominal read and write cycles of 280 and 380 nanoseconds, respectively. The basic 65K-word storage unit consists of four 16K modules, and may be expanded by four modules to a capacity of 131K words per storage unit. The minimum primary storage for a basic 1x1 configuration (one CAU and one IOAU) is a 32K word storage unit consisting of four 8K modules. A total of four 131K units provide a maximum primary storage capacity of 524K words in a system. The basic (nonexpanded) 32K or 65K storage unit accommodates sixteen access paths, servicing four of them simultaneously; an expanded 65K or 131K unit accommodates up to sixteen access paths, servicing eight of them simultaneously. Partial (sixth, quarter, third, and half) as well as full-word operation is provided.

2.2.6. Extended Storage

The second level of directly addressable main storage in the 1100/40 Systems is the extended storage system. The minimum extended storage configuration consists of 131K 36-bit words. Extended storage capacity may be expanded in 131K increments up to a maximum of 1048K 36-bit words. Each unit has a 800 nanosecond read/write cycle. Extended storage is connected to the system by multiple access interface (MAI) units which provide up to ten access paths to each storage unit which will accommodate the largest 1100/44 configuration.

2.2.7. Maintenance Controller

The maintenance controller provides for diagnostic checkout by the automatic comparison of maintenance panel indicators against known good data on tape for the following:

- Command/Arithmetic Units
- Input/Output Access Units
- Disc Controllers
- Communication/Symbiont Processor
- Printer circuit cards

To complement its diagnostic capability, the maintenance controller allows for the operation of the operator/ maintenance panels by personnel at a remote site via communications lines (Remote Communications Interface).

2.2.8. Auxiliary Storage and Peripheral Subsystems

The 1100/40 Systems offer a full range of peripheral subsystems; this wide range provides the capability to satisfy many requirements. The standard Sperry Univac peripheral subsystems include:

- SPERRY UNIVAC 8405 Disc Subsystem
- SPERRY UNIVAC 8430 Disc Subsystem
- SPERRY UNIVAC 8433 Disc Subsystem
- SPERRY UNIVAC 8425 Disc Subsystem
- UNISERVO 12/16 Magnetic Tape Subsystem
- UNISERVO 20 Magnetic Tape Subsystem
- FH–432/1782 Drum Subsystem
- SPERRY UNIVAC 0770 High Speed Printer Subsystem
- SPERRY UNIVAC 0716 Card Reader Subsystem
- SPERRY UNIVAC 0604 Card Punch Subsystem
- SPERRY UNIVAC DCT 500 Data Communications Terminal
- SPERRY UNIVAC DCT 1000 Data Communications Terminal
- UNISCOPE 100 Display Terminal
- UNISCOPE 200 Display Terminal

- Communications/Symbiont Processor (C/SP)

- General Communications Subsystem (GCS)

- Remote SPERRY UNIVAC 9200/9300 Subsystem

2.2.9. Destandardized Subsystems

Auxiliary storage and peripheral subsystems used on earlier model SPERRY UNIVAC 1100 Series Systems can be configured, but Sperry Univac will not develop any new software for these destandardized subsystems.

2.3. CONFIGURATION

The basic 1100/41 System (1x1 configuration) consists of two functionally and physically independent units: one CAU and one IOAU. The processor organization is intrinsically that of a multi-task processor and is designed for operation in a multiprogramming environment. The basic processor may be expanded by adding CAUs and/or IOAUs up to a total of four CAUs and four IOAUs (4x4). The basic 1100/41 system (1x1 configuration) is shown in Figure 2–1; Table 2–1 lists all fully supported configurations. The fully supported configurations are: 1100/41 System (1x1 configuration), 1100/42 System (2x1 or 2x2 configuration), 1100/43 System (3x2 or 3x3 configuration), and the 1100/44 System (4x2, 4x3, or 4x4 configuration).

2.3.1. Minimum Peripheral Complement

The following list of peripheral equipment is the minimum available with the 1100/40 Systems. This minimum has been established to ensure an adequate complement for customer engineering and software support.

MINIMUM PERIPHERAL COMPLEMENT:

- One SPERRY UNIVAC Magnetic Disc Subsystem with: one 8430 Disc Unit, one 8433 Disc Unit, or two 8425 Disc Units.

- One UNISERVO Magnetic Tape Subsystem with: four UNISERVO 12, four UNISERVO 16, or four UNISERVO 20 Magnetic Tape Units.

- One SPERRY UNIVAC 0770 Printer and one SPERRY UNIVAC 0716 Card Reader operating via MSA or C/SP.

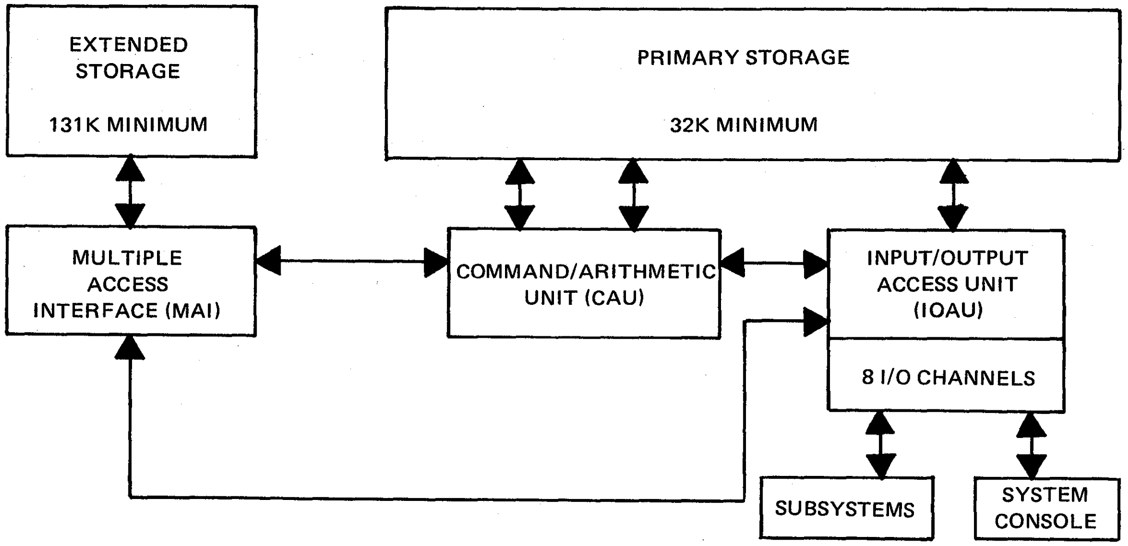


Figure 2–1. SPERRY UNIVAC 1100/41 System, Basic Configuration (1x1)

Table 2–1. Fully Supported Configurations

UNITS	CONFIGURATION							
	1100/41 1x1	1100/42 2x1	1100/42 2x2	1100/43 3x2	1100/43 3x3	1100/44 4x2	1100/44 4x3	1100/44 4x4
CAU	1	2	2	3	3	4	4	4
IOAU	1	1	2	2	3	2	3	4
PRIMARY STORAGE (words)	32K–524K	65K–524K	65K–524K	131K–524K	131K–524K	131K–524K	131K–524K	131K–524K
EXTENDED STORAGE (words)	131K–1048K	262K–1048K	262K–1048K	262K–1048K	262K–1048K	262K–1048K	262K–1048K	262K–1048K
MAI	1–8	2–8	2–8	2–8	2–8	2–8	2–8	2–8
SYSTEM CONSOLE	1–4	1–4	2–4	2–4	2–4	2–4	2–4	2–4
SYSTEM PARTITIONING UNIT	0–1	0–1	0–1	1	1	1	1	1

3. COMMAND ARITHMETIC UNIT

3.1. GENERAL

The command/arithmetic unit (CAU) is a multitask instruction stacking processor maintaining control over the arithmetic and instruction sequencing operations in the SPERRY UNIVAC 1100/40 System. All CAUs are capable of interfacing with a maximum of four primary storage units (524K 36-bit words). Independent instruction and operand paths are provided for each primary storage unit; each CAU is also capable of interfacing with multiple access interface (MAI) units for up to 1048K words of extended storage. The paths to extended storage have overlapping capability which permits faster effective cycle time.

The CAU generates interrupt signals on any one of three interprocessor interrupt lines and receives interprocessor interrupt signals from a maximum of three sources. The CAU is capable of controlling one or two IOAUs. Each CAU includes five interacting components which are described in 3.1.1 through 3.1.5. Figure 3—1 illustrates the configuration of the command/arithmetic unit.

3.1.1. Address Formation Section

The relative and absolute operand and absolute instruction addresses are formed in this section. During the operand address generation cycle, possible storage conflicts are checked, the base address is formed, program limits are checked, and index incrementation is performed.

The 18-bit relative operand address is formed by adding the contents of the modifier portion of the specified index register to the u-field of the instruction. The 24-bit absolute address is formed by adding the contents of the index register specified in the instruction, the u-field of the instruction, and the contents of a 15-bit base (instruction base or data base) from the processor state register.

The instruction address section accepts a 24-bit absolute address from the address formation section. The proper request is then formed to accompany the address to the proper storage module. The address is increased by one, and upon receipt of the proper acknowledge, the next request is sent to storage. Instruction referencing continues for consecutive addresses until a jump instruction is executed or an interrupt disrupts the sequence. In the case of a jump, a new absolute address is received from the operand addressing section, and the instruction referencing sequence is reinitiated.

3.1.2. General Register Stack (GRS)

The general register stack (GRS) consists of 112 integrated circuit control registers, program-addressable, each with a capacity of 36 bits. The GRS includes indexing registers, accumulators, repeat counters, a mask register, a real time clock register, and temporary storage locations for the processor state register. The stack is divided into an odd/even structure to allow simultaneous referencing when double-precision 72-bit word instructions are used.

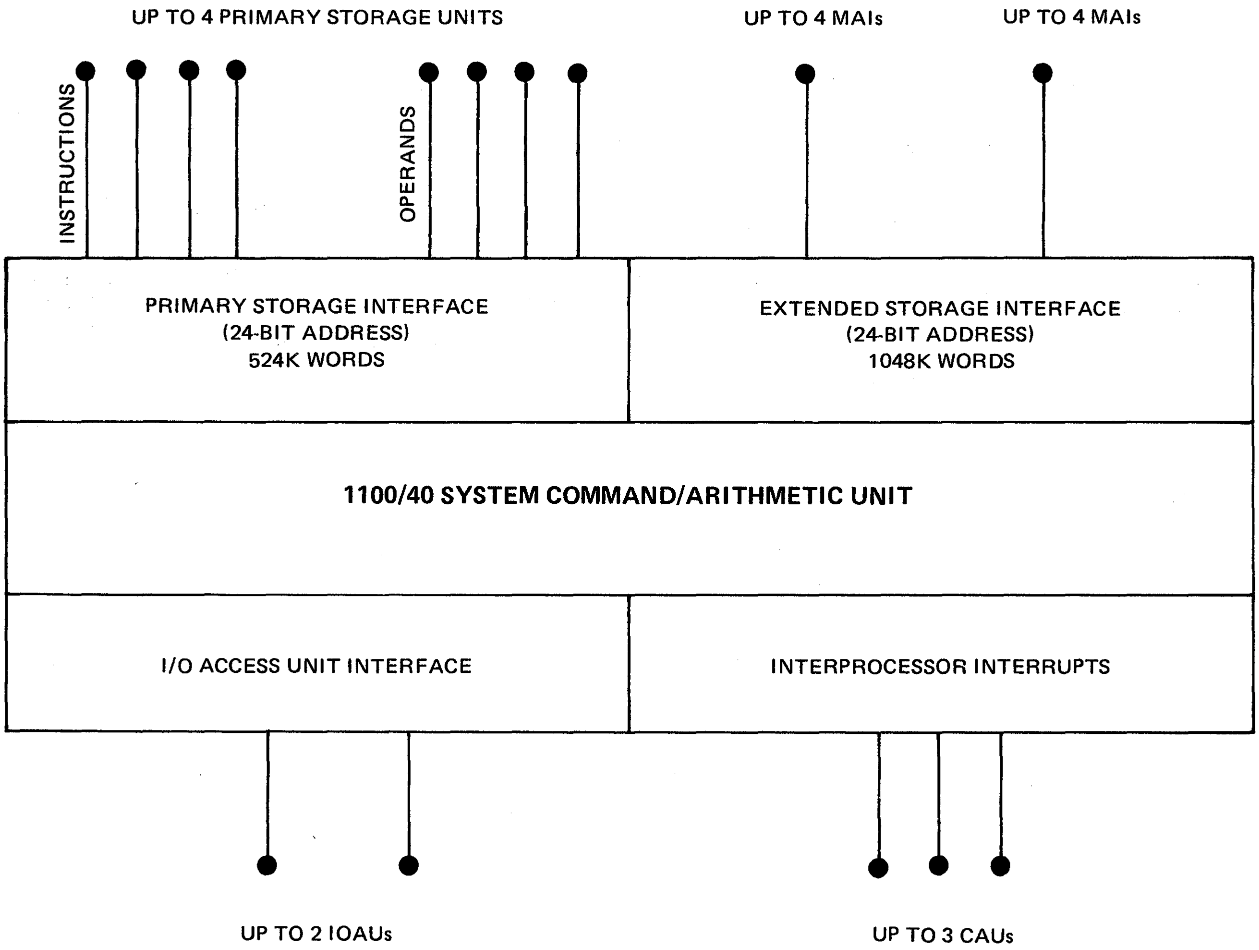

UP TO 4 PRIMARY STORAGE UNITS
UP TO 4 MAIs
UP TO 4 MAIs
INSTRUCTIONS
OPERANDS
PRIMARY STORAGE INTERFACE
(24-BIT ADDRESS)
524K WORDS
EXTENDED STORAGE INTERFACE
(24-BIT ADDRESS)
1048K WORDS
1100/40 SYSTEM COMMAND/ARITHMETIC UNIT
I/O ACCESS UNIT INTERFACE
INTERPROCESSOR INTERRUPTS
UP TO 2 IOAUs
UP TO 3 CAUs

Figure 3–1. Command/Arithmetic Unit Configuration

The executive, through modes established in the processor state register, has exclusive use of a duplicate set of control registers.

3.1.3. Conditional Jump Section

The conditional jump section minimizes execution time in the CAU when a conditional jump instruction is encountered. This section, divorced from the main arithmetic section, tests whether the jump conditions are satisfied before control passes to the arithmetic section.

3.1.4. Store Operation Section

The store operation section, a subdivision of the control section of the CAU, handles all writing into storage. This section performs operations necessary for full-word and partial-word transfers into storage.

3.1.5. Arithmetic Section

In the 1100/40 System, the manipulation of data (addition, subtraction, multiplication, division, shifting) takes place in the arithmetic section of the CAU. During the execution of an arithmetic instruction, nonaddressable transient storage registers within the arithmetic section are used for the actual computation. The arithmetic section has the following capabilities:

- For fixed-point single-precision instructions, the j-designator selects all of a word or a portion (half, third, quarter, or sixth) of a word for use in the arithmetic operation.
- By using special split-word arithmetic instructions, simultaneous addition or subtraction of corresponding half- or third-words is done.
- Through the use of a shift matrix, multiposition shifts require the same time as single bit position shifts. Right and left shifts of single- or double-word operands can be specified. Left shifting may be circular or logical. Right shifts may be circular, logical, or algebraic. When the results of an arithmetic operation are in double-word 72-bit form they are automatically stored in consecutive control registers and may be retrieved as 72-bit length results or operands.
- Alphanumeric comparisons utilizing the mask register (R2) allow any selection of bits in one 36-bit word to be directly compared with the corresponding bits of another word or series of words.

3.1.5.1. The Adder

The adder in the CAU is a ones complement subtractive adder for 36-bit and 72-bit operations. For purposes of analysis and debugging, the programmer may manually simulate the processor operations by simple binary or octal addition.

Two special internal designators associated with the arithmetic adder are the overflow and carry designators. The fixed-point addition and subtraction instructions, single and double precision, and the Load Processor State Register instruction are the only instructions which affect these two designators.

3.1.5.2. Arithmetic Accumulators

The 16 arithmetic accumulators in the GRS can be addressed directly by the programmer and are used to hold operands and results of arithmetic computations. These arithmetic accumulators should not be confused with the nonaddressable transient registers that are used in actual computation and are contained within the arithmetic section itself.

With the Add to X and Add Negative to X instructions, the index registers also act as accumulators in the same manner as the arithmetic registers.

3.1.5.3. Partial-Word Transfers

To minimize shifting and masking and to allow computation based on selected portions of words, the 1100/40 System permits the transfer of partial words into and out of the arithmetic section in a varying pattern (see Table 3—1).

By selecting the coding of the j-designator in the instruction word and the quarter-word mode designator of the processor state register, a programmer may transfer a chosen portion of an operand to or from a control register or the arithmetic section. The transfer to an arithmetic register may also be accompanied by sign extension for subsequent arithmetic operations, depending on the j-designator.

Table 3—1. j-Determined Partial-Word Operation

j (Octal)	PSR Bit 17	Bit Positions of (U) → A, X, or R	Bit Positions of (A), (X), or (R) → U
00	–	35–00 → 35–00	35–00 → 35–00
01	–	17–00 → 17–00	17–00 → 17–00
02	–	35–18 → 17–00	17–00 → 35–18
03	–	17–00 → S 17–00	17–00 → 17–00
04**	0	35–18 → S 17–00	17–00 → 35–18
	1	26–18 → 08–00	08–00 → 26–18
05**	0	11–00 → S 11–00	11–00 → 11–00
	1	08–00 → 08–00	08–00 → 08–00
06**	0	23–12 → S 11–00	11–00 → 23–12
	1	17–09 → 08–00	08–00 → 17–09
07**	0	35–24 → S 11–00	11–00 → 35–24
	1	35–27 → 08–00	08–00 → 35–27
10	–	05–00 → 05–00	05–00 → 05–00
11	–	11–06 → 05–00	05–00 → 11–06
12	–	17–12 → 05–00	05–00 → 17–12
13	–	23–18 → 05–00	05–00 → 23–18
14	–	29–24 → 05–00	05–00 → 29–24
15	–	35–30 → 05–00	05–00 → 35–30
16	–	18 bits* → 17–00	NO TRANSFER
17	–	18 bits* → S 17–00	NO TRANSFER

*If $x = 0$: h, i, and u are transferred. If $x \neq 0$: $u + (X_x)_m$ is transferred.

**These values reference control registers when character addressing mode is set in the PSR.

S = Sign extension, where the sign is the leftmost bit of the partial word selected by j.

3.1.5.4. Split-Word Arithmetic

The system can perform addition and subtraction of half-words or third-words simultaneously. The right halves of two operands, for example, are added and the sum is stored in the right half of the selected accumulator. At the same time, the left halves of the same two operands are added and the result is stored in the left half of the same accumulator. There is no carry interaction between the halves. The same holds true for thirds of words. Each partial word operates as an independent entity with its own end-around carry.

3.1.5.5. Shifting

The 1100/40 System can perform both single-length shifting (36 bits) or double-length shifting (72 bits), treating the latter as if operating with a single 72-bit register. A high-speed shift matrix makes execution time independent of the number of places involved in the shift, which means that an operand can be shifted from 0 to 72 positions in one storage cycle time.

Six types of shift operations are provided:

- Right Circular – bits shifted out at the right reappear at the left.
- Left Circular – bits shifted out at the left reappear at the right.
- Right Logical – zeros replace bits shifted out of the most significant positions. Bits shifted out of the least significant position are lost.
- Left Logical – zeros replace bits shifted out of the least significant positions. Bits shifted out of the most significant position are lost.
- Right Algebraic – sign bits replace bits shifted out of the most significant positions. Bits shifted out of the least significant position are lost.
- Scale-Factor Shift – a single or double accumulator left shift which positions the word and simultaneously counts the number of shifts required until the most significant bit of the accumulator is different than the next most significant bit.

3.1.5.6. Double-Precision Fixed-Point Arithmetic

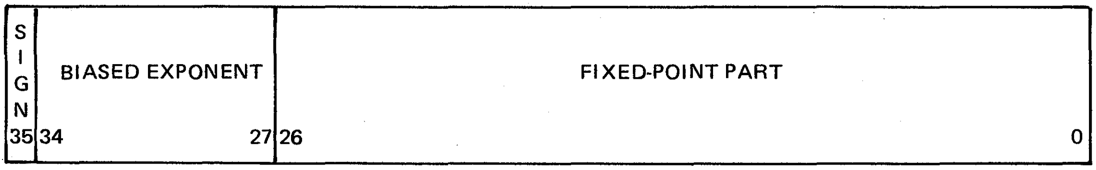
The 1100/40 System provides 72-bit, double-precision fixed-point addition and subtraction. Operands are processed as if they occupied a single 72-bit register. Bit 71, the high order bit, is the sign bit.

In addition, several arithmetic instructions produce two-word results. With fixed-point multiplication, a double-length product is stored in two arithmetic registers for integer and fractional operations. Integer and fractional division is performed upon a double-length dividend with the quotient retained in A and the remainder retained in A + 1.

3.1.5.7. Floating-Point Arithmetic

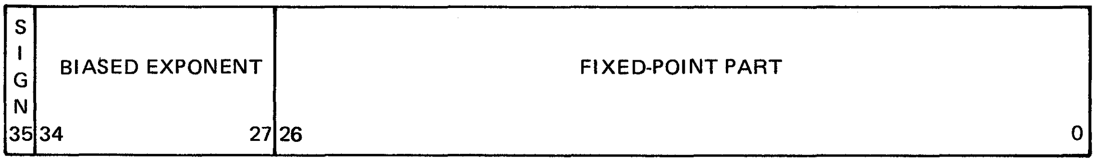
The 1100/40 System provides an extensive hardware repertoire of floating-point instructions. If the arithmetic is single precision, the range is from 10^{38} to 10^{-38} with eight-digit precision. The word formats are given below.

Source Format:

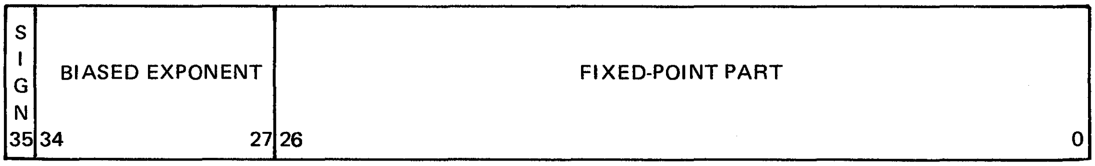


Result Format:

WORD 1



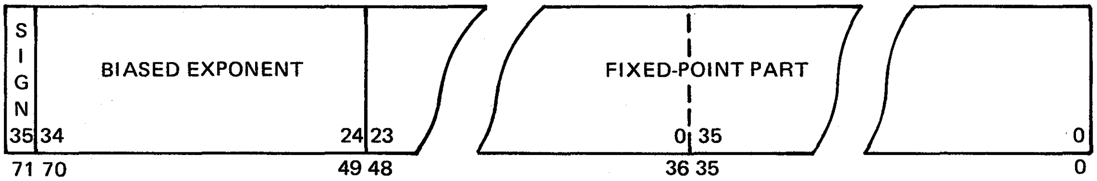
WORD 2



In a single-precision floating-point operation, word 1 is the more significant portion of the result. Word 2 contains the less significant portion. Mathematical error tracing can determine how much accuracy is being lost in calculations using this format. The two-word result of these single-precision operations is developed in two contiguous arithmetic registers. The storing of the second result word may be inhibited under program control to speed operations.

Double-precision floating-point operands and results fall into the approximate range of 10^{307} to 10^{-308} with 18-digit precision. The values are expressed in two adjacent words as shown in the following format.

Source and Result Format:



Full double-precision operations do not require a repeated sign and exponent in the 36 least significant bits.

To express negative exponents, the hardware biases (floats) the exponent on a midvalue. The sign bit of the floating-point word applies to the fixed-point part. The true and biased ranges of the exponent are as follows:

	True	Biased
Single-precision (8 bits)	-128_{10} to $+127_{10}$	$0 - 255_{10}$
Double-precision (11 bits)	-1024_{10} to $+1023_{10}$	$0 - 2047_{10}$

The fixed-point part of a floating-point number is normally in the range from 1/2 to 1. Such a value places a 1 bit in the most significant bit position of the fixed-point part. When this condition exists, the floating-point number is said to be normalized. A negative floating-point number is represented by the ones complement of the entire corresponding positive floating-point number.

Floating-point instructions are also provided for the following operations:

- Determining differences in exponents
- Packing and unpacking exponents and fixed-point parts (single- and double-precision)
- Conversion — Single- to double-precision
  Double- to single-precision

3.2. INSTRUCTION STACKING

The CAU uses the instruction stacking technique to control up to four instructions at various stages of execution. Instruction execution generally involves a series of five basic operations:

- Instruction acquisition sequence
- Address generation sequence
- Operand acquisition sequence
- Computational sequence
- Results storage sequence

As a result of the four-deep instruction stack and dual data path arrangements, these sequences may be initiated such that the effective instruction execution time per non-extended sequence instruction is 300 nanoseconds.

Figure 3—2 shows a cross section in time of an instruction stream flowing through the CAU.

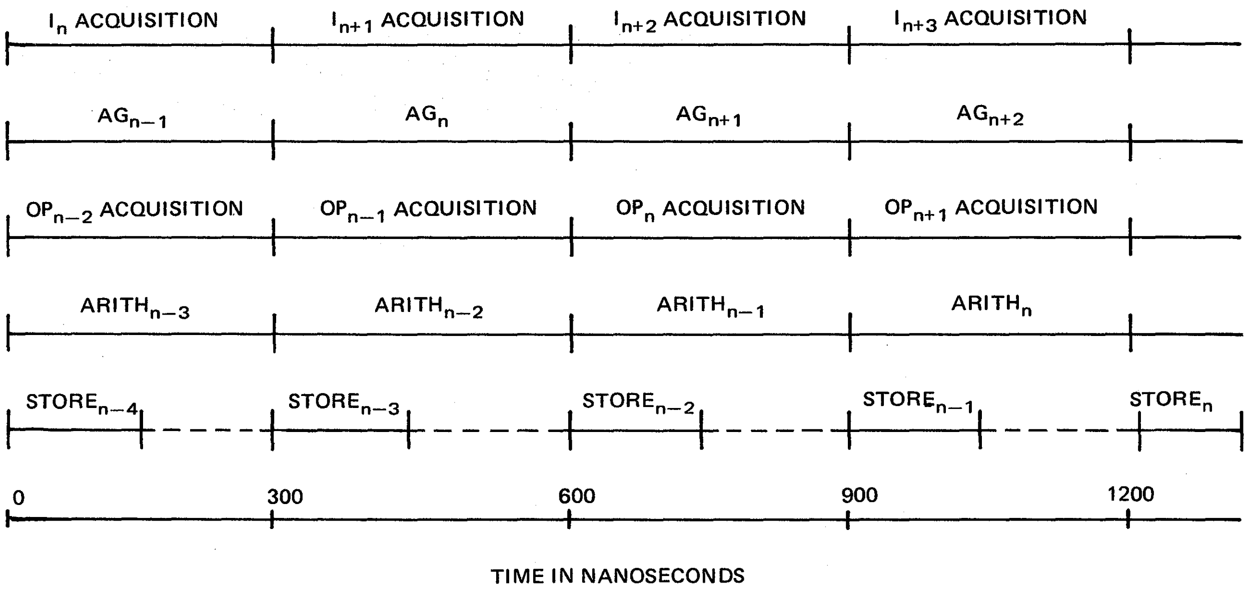


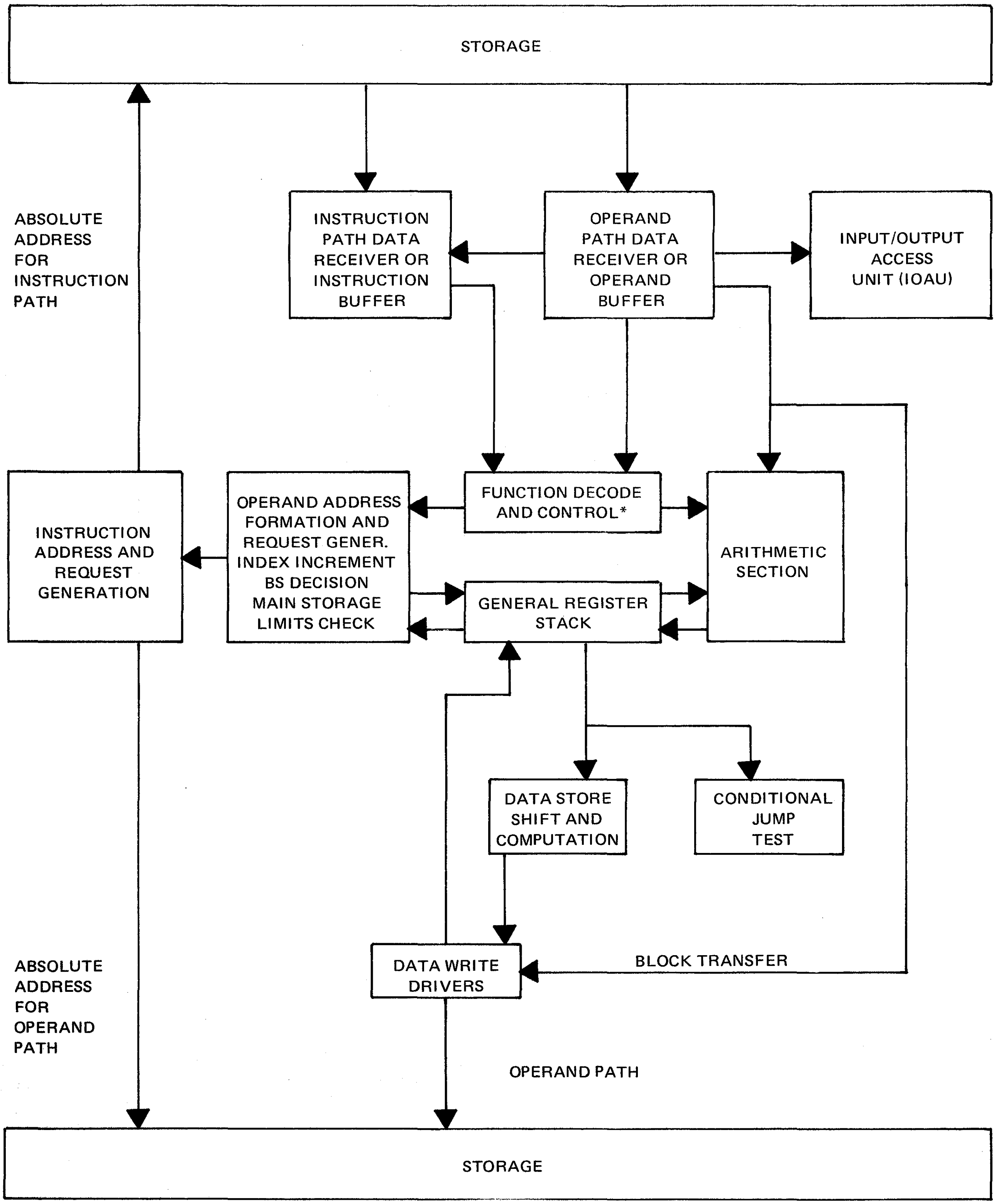
Figure 3–2. Instruction Execution (Approximate Timing) in a Command/Arithmetic Unit

3.3. OPERATIONS IN BRIEF

A block diagram of CAU operations is given in Figure 3–3. Instructions to be interpreted are routed to the function decode and control section from either the instruction path from storage, the instruction buffer, the operand path, or the operand buffer. The route taken depends upon the initial reference and state of the processing section.

If reading data from storage is necessary for the execution of the instruction, an absolute operand address is formed and the proper data is requested. Upon receipt of the data, the arithmetic section performs the required operation; the results of the operation are temporarily stored.

The arithmetic section is bypassed if the instruction requires only writing data into storage. In this case, from the function and decode section, the instruction is passed to the general register stack (GRS). From the GRS, data is passed through the store section and written into storage.


STORAGE
ABSOLUTE ADDRESS FOR INSTRUCTION PATH
INSTRUCTION PATH DATA RECEIVER OR INSTRUCTION BUFFER
OPERAND PATH DATA RECEIVER OR OPERAND BUFFER
INPUT/OUTPUT ACCESS UNIT (IOAU)
INSTRUCTION ADDRESS AND REQUEST GENERATION
OPERAND ADDRESS FORMATION AND REQUEST GENER. INDEX INCREMENT BS DECISION MAIN STORAGE LIMITS CHECK
FUNCTION DECODE AND CONTROL*
ARITHMETIC SECTION
GENERAL REGISTER STACK
DATA STORE SHIFT AND COMPUTATION
CONDITIONAL JUMP TEST
ABSOLUTE ADDRESS FOR OPERAND PATH
DATA WRITE DRIVERS
BLOCK TRANSFER
OPERAND PATH
STORAGE

*Control may pass directly to the input/output access unit

Figure 3–3. Instruction Path Through the Command/Arithmetic Unit

3.4. INSTRUCTION WORD FORMAT

The format of the 1100/40 System instruction word is illustrated below followed by an explanation of each field. Some fields have more than one meaning, depending on the class of instruction.

f	j	a	x	h	i	u
35 30	29 26	25 22	21 18	17	16	15 0

3.4.1. Function Code – f-Field

These six bits specify the operation to be performed. For function codes above 70_8, the f- and j-fields are combined to produce a 10-bit function code. An invalid function code generates an interrupt.

3.4.2. Partial-Word or Immediate-Operand Designator – j-Field

For function codes less than 70_8, the 4-bit j-field specifies partial-word or immediate-operand selection (see Table 3–1 for specific partial-word selections) or a control register when character addressing mode is set in the PSR (see 6.7).

3.4.3. Control Register Designator – a-Field

The four-bit a-field designates which control register, within a group selected by the function code, is involved in the operation. For most operations, the a-field refers to an arithmetic register; for a few, it refers to either an index register or some other control element. In input/output instructions, it is used in specifying the channel and its associated input or output access control register. For function code 70_8, the a- and j-designators together address one of the 112 control registers.

3.4.4. Index Register Designator – x-Field

The 4-bit x-field specifies one of the 15 index registers to be used in address modification. When x = 0 is designated, indexing is suppressed.

3.4.5. Index Modification Designator – h-Field

The 1-bit h-field controls modification of the index value (X_m) by the increment field (X_i) after indexing (see 3.5.1). If h = 1, the right half of the index register is modified by adding the contents of its left half; if h = 0, modification is suppressed.

3.4.6. Indirect Address Designator – i-Field

The 1-bit i-field normally controls the use of indirect addressing during instruction execution. If i = 0, the instruction functions without indirect addressing. If i = 1, the 22 least significant bit positions of the instruction (x-, h-, i-, and u-fields) are normally replaced in the instruction register with the contents of the 22 least significant bit positions of the word at the effective address. Indirect addressing continues as long as i = 1 with full indexing capability at each level.

3.4.7. Address Field – u-Field

The u-field normally specifies the operand address. However, for certain instructions it may hold a constant. For example, the shift instructions use the seven least significant bit positions to produce the shift count. For all instructions, the value in the u-field may be modified by the contents of an index register. It may also be used as part of the indirect address designator.

3.5. GENERAL REGISTER STACK (GRS)

The GRS (Figure 3–4) includes 112 program-addressable control registers which consist of 36-bit integrated-circuit registers, with a basic cycle time of 90 nanoseconds. Four parity bits are included with each control register.

Effective use of multiple accumulators and index registers for the development and use of constants, index values, and operands substantially improves performance. Four of the accumulators (A registers) overlap four of the index registers (X registers) which provides additional versatility in the use of these registers.

In the following descriptions only programmable registers are discussed. The executive, through modes established by the contents of the processor state register, has exclusive use of the duplicate set of control registers indicated by the shaded areas in Figure 3–4, as well as the associated registers in the IOAU.

3.5.1. Index Registers

Control register locations 1_8 – 17_8 are index registers and normally have the following format:

X_i MODIFIER INCREMENT OR DECREMENT 35 18	X_m INDEX MODIFIER 17 0

The X_m portion of the index register is an 18-bit modifier to be added to the base operand address of the instruction. The X_i portion of the index word updates the X_m portion, *after* base operand address modification.

Index register modification is specified by a 1 bit in the h-field of the instruction, while indexing itself is specified by a nonzero value in the x-field. Both functions take place within the basic instruction execution cycle.

When cascaded indirect addressing is used in a programmed operation, full indexing capabilities are provided at each level. Indirect addressing replaces the x-, h-, i-, and u-fields of the instruction register, beginning with a new indexing cycle for each cascaded sequence. This process continues until the i-field is zero.

3.5.2. Arithmetic Accumulators

Control register locations 14_8 – 33_8 are arithmetic accumulators for programmed storage of arithmetic operands and results. The actual computation is performed in nonaddressable transient registers within the arithmetic section.

Depending upon the instruction, use of the accumulators results in a variety of word formats. Double-precision instructions and a number of logical instructions reference two contiguous accumulators, that is, A and A+1. In arithmetic operations requiring two-word operands or producing two-word results, A+1 always holds the least significant part of an operand or result. Some instructions, such as single-precision floating-point operations, call on a one-word operand from main storage but produce a two-word result in the specified A and A+1.

OCTAL		DECIMAL	
0	NONINDEXING REGISTER (X0)	0	UNASSIGNED
1 13	Xi Xm	1 11	15 INDEX REGISTERS (X)
14 17		12 15	4 OVERLAPPED (X OR A)
20 33		16 27	16 ACCUMULATORS (A)
34 37		28 31	4 UNASSIGNED
40	PROCESSOR STATE REGISTER (MAIN)	32	TEMPORARY STORAGE FOR 4 PROCESSOR STATE REGISTERS
41	TEMPORARY STORAGE	33	
42	PROCESSOR STATE REGISTER	34	
43	(UTILITY) TEMPORARY STORAGE	35	
44	EXEC BANK DESCRIPTOR POINTER REGISTER	36	2 BANK DESCRIPTOR POINTER REGISTERS
45	USER BANK DESCRIPTOR POINTER REGISTER	37	
46	CURRENT BANK DESCRIPTOR INDEXES (PACKED) FOR MAIN PSR	38	2 BANK DESCRIPTOR INDEXES
47	CURRENT BANK DESCRIPTOR INDEXES (PACKED) FOR UTILITY PSR	39	
50	UNASSIGNED	40	UNASSIGNED
51	STORAGE PARITY CHECK STATUS WORD	41	5 INTERRUPT STATUS WORDS
52	INTERFACE PARITY CHECK STATUS WORD	42	
53	GUARD MODE INTERRUPT STATUS WORD	43	
54	UNDEFINED SEQUENCE INTERRUPT STATUS WORD	44	
55	SYSTEM INTERRUPT STATUS WORD	45	
56	PRIMARY STORAGE REFERENCE COUNTER	46	2 STORAGE REFERENCE COUNTERS
57	EXTENDED STORAGE REFERENCE COUNTER	47	
60 77	NOT USABLE	48 63	IS NOT USABLE
100	REAL TIME CLOCK (R0)	64	16 SPECIAL REGISTERS (R)
101	REPEAT COUNT REGISTER (R1)	65	
102	MASK REGISTER (R2)	66	
103 105	R3–R5 STAGING REGISTERS OR SR1–SR3	67 69	
106 111	R6–R9 J-REGISTERS OR J0–J3	70 73	
112 117	UNASSIGNED (R10–R15)	74 77	
120	UNASSIGNED (R0)	80	16 SPECIAL REGISTERS (R)
121	REPEAT COUNT REGISTER (R1)	81	
122	MASK REGISTER (R2)	82	
123 125	R3–R5 STAGING REGISTERS OR SR1–SR3	83 85	
126 131	R6–R9 J-REGISTERS OR J0–J3	86 89	
132 137	UNASSIGNED (R10–R15)	90 95	
140	NONINDEXING REGISTER (X_0)	96	UNASSIGNED
141 153	Xi Xm	97 107	15 INDEX REGISTERS (X)
154 157		108 111	OVERLAPPED (X OR A)
160 173		112 123	16 ACCUMULATORS (A)
174 177	UNASSIGNED	124 127	4 UNASSIGNED

36 BIT + PARITY

▨ For executive use only (guard mode protected)

Figure 3–4. General Register Stack (GRS)

3.5.3. R Registers

The sixteen control register locations 100_8 – 117_8 are R registers. The first three of these (R0, R1, R2) have specified functions and formats as described below. The remaining R registers are not specifically assigned; typically they are used as loop counters, transient registers, or storage for intermediate values or constants. R3, R4, and R5 are used as staging registers (SR1, SR2, SR3) in character instructions. R6 through R9 are used as J registers when the character addressing mode is set in the processor state register (see 4.2).

3.5.3.1. R0 – Real Time Clock

UNASSIGNED	CLOCK COUNT
35 18	17 0

This register is initially loaded by the program. The contents are then decremented once each 200 microseconds. A real time clock interrupt occurs when the clock count is decremented through zero. Thus, if the clock is initially loaded with the value 5000, an interrupt occurs in exactly one second.

3.5.3.2. R1 – Repeat Counter

UNASSIGNED	REPEAT COUNT (k)
35 18	17 0

The repeat counter controls repeated operations such as block transfer and search instructions. To execute a repeated instruction k times, the repeat counter is loaded with k prior to the execution of the instruction.

3.5.3.3. R2 – Mask Register

The mask register functions as a filter in determining which portions of words are to be compared in repeated masked search operations. The mask register must be loaded prior to executing the search command. The contents of the effective address are compared to the contents of the arithmetic register only with respect to those positions which contain one's in the mask register.

3.6. INSTRUCTION REPERTOIRE

The 1100/40 System is provided with an unusually powerful and flexible instruction repertoire. Many of the instructions are effectively accessed and completed in the time of one storage cycle. Included in the complete set of instructions is a group which permits fast and simplified executive system control.

To a great extent, the instruction repertoire of the 1100/40 System is identical to that of other SPERRY UNIVAC 1100 Series Systems in order to maintain total compatibility. To utilize the greater capacity of the 1100/40 System, character manipulation instructions and additional privileged instructions have been included.

The following sections group the instructions by functional class to illustrate the scope of the 1100/40 instruction repertoire.

3.6.1. Load Instructions

Single-precision load instructions cause transfers from storage through the arithmetic unit according to the j-designator value to the register designated by the a-field.

Double-precision load instructions use the j-field as a minor function code designator.

The load instructions are:

Load A
Load Negative A
Load Magnitude A
Load Negative Magnitude A
Load R
Load X
Load X Modifier
Load X Increment
Double Load A
Double Load Negative A
Double Load Magnitude A

3.6.2. Store Instructions

The contents of the A, R, and X registers specified by the a-field are transferred to a storage location under j-designator control. If U is less than 200_8, the complete data word is transferred to a control register in the general register stack. The Store Zero instruction stores zeros at location U. The Block Transfer instruction moves a block of information in storage. The number of words transferred is defined by the repeat count stored in the repeat count register.

The store instructions are:

Store A
Store Negative A
Store Magnitude A
Store R
Store Zero
Store X
Block Transfer
Double Store A

3.6.3. Fixed-Point Arithmetic Instructions

Add or Add Negative instructions add or subtract the contents of U from specified A or X registers. The transfer of data from location U to the arithmetic unit is under control of the j-designator. For double-precision and parallel half-word and third-word arithmetic operations, the value in the j-field is a minor function code.

The sign of the product or quotient of multiply and divide instructions is determined by algebraic rules; operands of like signs produce a positive result and operands of unlike signs produce a negative result.

The fixed-point arithmetic instructions are:

Add to A
Add Negative to A
Add Magnitude to A
Add Negative Magnitude to A
Add Upper
Add Negative Upper
Add to X
Add Negative to X
Multiply Integer
Multiply Single Integer
Multiply Fractional
Divide Integer
Divide Single Fractional
Divide Fractional
Double-Precision Fixed-Point Add
Double-Precision Fixed-Point Add Negative
Add Halves
Add Negative Halves
Add Thirds
Add Negative Thirds

3.6.4. Floating-Point Arithmetic Instructions

Floating-point arithmetic instructions cause the transfer of single- or double-precision operands from storage to the arithmetic unit. The j-field is a minor function code designator. The single-precision floating-point operations of Add, Add Negative, Multiply, and Divide instructions produce results consisting of two single-precision words which are: sum and residue, difference and residue, the most and least significant position of the double length product, and quotient and remainder, respectively. The storing of the second result word may be inhibited under program control to speed operation.

When a double-precision floating-point Add, Add Negative, Multiply, Divide, or Load and Convert to Floating instruction, or a Floating Expand and Load instruction is executed, and the mantissa of the double-precision result is +0 or −0, all 72 bits of the final result are cleared to zeros; a characteristic overflow or underflow interrupt never occurs.

If the floating-point Floating Compress and Load instruction is executed and the double-precision input operand has a +0 or −0 mantissa, the final result is cleared to all zeros.

Input operands for floating-point Multiply and Divide, Floating Expand and Load, and Floating Compress and Load instructions must be normalized.

The floating-point arithmetic instructions are:

Floating Add
Floating Add Negative
Floating Multiply
Floating Divide
Load and Unpack Floating
Load and Convert to Floating
Magnitude of Characteristic Difference to Upper

Characteristic Difference to Upper
Double Precision Floating Add
Double Precision Floating Add Negative
Double Precision Floating Multiply
Double Precision Floating Divide
Double Load and Unpack Floating
Double Load and Convert to Floating
Floating Expand and Load
Floating Compress and Load

3.6.5. Repeated Search Instructions

The repeated search instructions require that a repeat count be loaded into a register designated for this purpose. If a search instruction is initiated when the repeat value is zero, the search instruction is effectively skipped. Otherwise, the contents of the A register specified by the a-field is transferred to the arithmetic unit, and the operation specified by the instruction is initiated; this involves decrementing the repeat count, transferring an operand to the arithmetic section, performing the specified comparisons, and incrementing the index register.

If the condition being sought is not fulfilled and the repeat count is not zero, the instruction is executed again. The instruction is repeated until the condition specified by the instruction is fulfilled or until the repeat count is decreased to zero. If the condition is fulfilled, the operation is terminated, the next instruction is skipped, and the following instruction is performed; otherwise, the next instruction is taken.

For masked search instructions, the repeat count is loaded and a mask value is preloaded into the register specified for that purpose. A logical AND is performed with individual mask bits and the register contents designated by the instruction.

The repeated search and masked search instructions are:

Search Equal
Search Not Equal
Search Less Than or Equal
Search Greater
Search Within Range
Search Not Within Range
Mask Search Equal
Mask Search Not Equal
Mask Search Less Than or Equal
Mask Search Greater
Masked Search Within Range
Masked Search Not Within Range
Masked Alphanumeric Search Less Than or Equal
Masked Alphanumeric Search Greater

3.6.6. Test (or Skip) Instructions

These instructions cause data to be transferred to the arithmetic section and tested as prescribed by the instruction. If the condition specified is fulfilled, a skip is performed; otherwise the next sequential instruction is executed.

The test instructions are:

Test Even Parity
Test Odd Parity
Test Less Than or Equal to Modifier
Test Zero
Test Nonzero
Test Equal
Test Not Equal
Test Less or Equal
Test Greater
Test Within Range
Test Not Within Range
Test Positive
Test Negative
Double Precision Test Equal

3.6.7. Shift Instructions

When performing shift instructions, the contents of the specified A register is moved left or right a specified number of bit positions. The shifted values are stored back into the same A registers.

There are three basic types of shift instructions: circular, logical, and algebraic. The shift count is specified by bit positions 6 through 0 of the u-field. If the shift count exceeds 72, the results are not defined.

In the shift and count instructions, the shift count is not controlled by the instruction word. Instead, the contents of a single-word operand (U) or a double-word operand (U, U+1) are transferred to the arithmetic unit where the register contents are scaled; the contents are shifted left circularly until the leftmost two bits are unequal. The scaled data is stored in the a-field designated A registers specified by the instruction and the count (of the number of shifts necessary to scale the data) is stored in the adjoining A register.

The shift instructions are:

Single Shift Circular
Double Shift Circular
Single Shift Logical
Double Shift Logical
Single Shift Algebraic
Double Shift Algebraic
Load Shift and Count
Double Load Shift and Count
Left Single Shift Circular
Left Double Shift Circular
Left Single Shift Logical
Left Double Shift Logical

3.6.8. Executive System Control Instructions

This group of instructions allows executive system control of programs operating in a multiprocessing or multiprogramming environment. These instructions are used for establishing the contents of the processor state register, storage limits boundaries, interrupt locations, initiation and control of I/O activity, interprocessor communication, and task assignment.

The executive system control instructions are:

Prevent All I/O Interrupts and Jump
Load Processor State Register
Load Main Processor State Register
Load Utility Processor State Register
Initiate Interprocessor Interrupt
Enable Storage Reference Counter
Clear and Enable Storage Reference Counter
Load/Store Main Storage Limits Register
Load/Store Utility Storage Limits Register
Set MSR (Select Interrupt Location)
Load Last Address Register
Enable/Disable Day Clock
Load Breakpoint Register
Store Jump Stack

3.6.9. Jump Instructions

Each of the conditional jump instructions performs a specific test. If the condition specified by the instruction exists, the instruction stored at address U is executed next; otherwise, the next sequential instruction is taken.

The Jump Greater and Decrement instruction forms a general register stack address from the combined j- and a-fields; the contents of this address is tested to determine if the jump will be made.

The conditional and unconditional jump instructions are:

Jump Greater and Decrement
Double Precision Zero Jump
Store Location and Jump
Jump Positive and Shift
Jump Negative and Shift
Jump Zero
Jump Nonzero
Jump Positive
Jump
Jump Keys
Halt Jump
Halt Keys and Jump
Allow All I/O Interrupts and Jump
Jump No Low Bit
Jump Low Bit
Jump Modifier Greater and Increment
Load Modifier and Jump

Jump Overflow
Jump No Overflow
Jump Carry
Jump No Carry
Jump Floating Overflow
Jump No Floating Overflow
Jump Floating Underflow
Jump No Floating Underflow
Jump Divide Fault
Jump No Divide Fault
Load I Bank Base and Jump
Load D Bank Base and Jump

3.6.10. Logical Instruction

The logical instructions perform logical AND, OR, and XOR operations. One of the operands is obtained from storage location U and the other from A. The logical result is placed in A+1.

The logical instructions are:

Logical OR
Logical XOR
Logical AND
Masked Load Upper

3.6.11. Miscellaneous Instructions

The Execute instruction allows the execution of an instruction at a remote address U without performing a jump to that address. The program address count is increased, and the instruction after the Execute instruction is performed next.

The Executive Return instruction allows a user to interrupt and switch control to the executive system.

The Test and Set instruction is used to test the entrance to areas of code that are not reentrant so as to be able to avoid attempting to share them simultaneously between CAUs. The 1100/40 System provides a skip in addition to an interrupt, using the a-field as a minor function code.

The miscellaneous instructions are:

Execute
Executive Return
No Operation (NO-OP)
Test and Set
Load/Store PSR Designators
Test and Set and Skip
Test and Clear and Skip

3.6.12. I/O Instructions

This group of instructions allows the program (usually the executive system) to initiate, test, and control the IOAU and its operations. If these instructions are executed while in the guard mode, a guard mode interrupt is generated.

The I/O instructions are:

Load Input Channel
Load Input Channel and Monitor
Jump Input Channel Busy
Disconnect Input Channel
Load Output Channel
Load Output Channel and Monitor
Jump Output Channel Busy
Disconnect Output Channel
Load Function Channel
Load Function Channel and Monitor
Jump Function in Channel
Allow All Channel External Interrupts
Prevent All Channel External Interrupts
Store Channel Number
Load Channel Select Register
Load Input Access Word
Load Output Access Word
Load Input Pointer Word
Load Output Pointer Word
Store Input Access Word
Store Output Access Word
Store Input Pointer Word
Store Output Pointer Word
Load Chain Base Register
Load Processor Interrupt Pointer Register
Allow Channel Interrupts
Prevent Channel Interrupts

3.6.13. Invalid and Unassigned Codes

Invalid operation codes generate an interrupt to location 241_8 when executed. The unassigned codes give unpredictable results when used and are reserved for future instruction repertoire expansion as are the invalid operation codes.

3.6.14. Character Instructions

The 1100/40 System provides a comprehensive subset of character-oriented data processing instructions. The instructions operate on strings of characters under the control of a set of three staging registers. The generation of addresses for the individual character strings utilizes both J registers and X registers. The J registers are implicitly addressed by the instructions and are used when indexing through the character strings. The x-field of the instruction specifies the first index register; additional index registers are X+1 and X+2, where X must be less than or equal to 15_8. The X registers are used to locate the individual character strings.

3.6.14.1. Byte Instructions

The byte instructions are:

Byte Move
Byte Move With Translate
Byte Translate and Test
Byte Translate and Compare
Byte Compare
Edit

3.6.14.2. Byte/Binary Conversion Instructions

The byte/binary conversion instructions are:

Byte to Packed Decimal Convert
Packed Decimal to Byte Convert
Byte to Binary Single Integer Convert
Byte to Binary Double Integer Convert
Binary Single Integer to Byte Convert
Binary Double Integer to Byte Convert
Byte to Single Floating Convert
Byte to Double Floating Convert
Single Floating to Byte Convert
Double Floating to Byte Convert
Quarter-Word Byte to Binary Compress
Binary to Quarter-Word Byte Extend
Quarter-Word Byte to Binary Halves Compress
Binary Halves to Quarter-Word Byte Extend
Quarter-Word Byte to Double Binary Compress
Double Binary to Quarter-Word Byte Extend

3.6.14.3. Decimal Arithmetic Instructions

The decimal arithmetic instructions are:

Byte Add
Byte Add Negative

3.7. STORAGE REFERENCE COUNTERS

The CAU includes two storage reference counters, one each for primary and extended storage. Each reference to storage made by a CAU will cause the appropriate storage reference counter to be incremented. These counters are for use by the executive system in storage and activity management. The storage reference counters are contained in the GRS (see Figure 3–2).

4. EXECUTIVE SYSTEM CONTROL FEATURES

4.1. GENERAL

The SPERRY UNIVAC 1100 Series Executive System, by use of special hardware features maintains complete control over the multiprogramming and multiprocessing environment of the SPERRY UNIVAC 1100/40 Systems.

The multiprogramming and multiprocessing capabilities of the 1100/40 Systems are based on guard mode operation. When operating in this mode, certain instructions, registers, and storage locations are available for the exclusive use of the executive. Under the guard mode, unrelated programs are protected from interacting or interfering with one another.

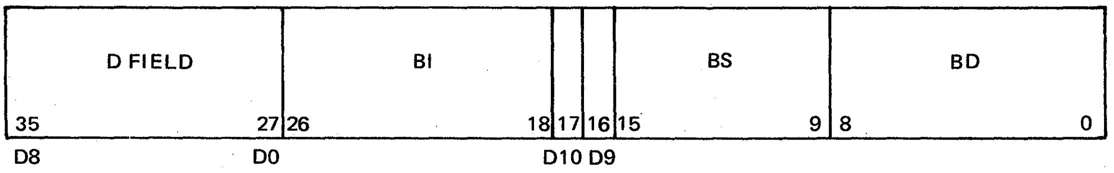
4.2. PROCESSOR STATE REGISTERS

Each command/arithmetic unit has two processor state registers (PSRs); a main PSR and a utility PSR. The PSRs are used to locate programs in any available storage area and to establish various operational modes. The PSRs are primarily controlled by the executive for itself and for user programs. The user is permitted to modify certain portions of a PSR by referencing a bank descriptor table (BDT) prepared by the executive for that program. The PSRs also record the arithmetic result status designators when an interrupt occurs. During an interrupt sequence, the contents of the PSRs are stored in the general register stack (GRS) and program control is transferred to the executive system.

The main processor state register is composed of two words called PSR and PSRE. A second processor state register, called the utility processor state register has the same format, except that the two words are called PSRU and PSRUE and designator bits are not used. The word formats of the main and utility PSRs follow.

Main Processor State Register Format

PSR



PSRE

UNUSED	D FIELD	BIX	BDX
35 25	24 12	11 6	5 0
	D23 D11		

PSR — first word of main PSR
PSRE — second word (extension portion) of main PSR
D FIELD — location of control designator bits D0 through D10 in PSR and D11 through D23 in PSRE
BI — I-bank base
BS — base selector
BD — D-bank base
D0 — carry designator
D1 — overflow designator
D2 — guard mode and storage protection
D3 — write only storage protection
D4 — character addressing mode
D5 — double-precision underflow
D6 — control register (GRS) selection
D7 — base register suppression (absolute addressing if D7 and the i bit of the instruction are both set)
D8 — floating point zero compatibility mode
D9 — index register mode selector (24 bit if set and D7 and the i bit of instruction are also set)
D10 — quarter-word mode
D11 — must be 0
D12 — PSR/SLR selector (PSRU and SLRU if set)
D13 — PSR I-bank write inhibit
D14 — PSR D-bank write inhibit
D15 — PSRU I-bank write inhibit
D16 — PSRU D-bank write inhibit

} guard mode fault interrupt occurs if write is attempted in a bank when the corresponding bit is set

D17 — enable floating-point residue
D18 — PSR and storage limits register auto-switch. When set allows switching from the currently active PSR and SLR, as specified by D12, to the inactive PSR and SLR if the storage limits test fails. For other than a jump, D12 remains in the same state.
D19 — executive BDP allow
D20 — enable arithmetic exception interrupt
D21 — floating underflow
D22 — floating overflow
D23 — divide fault
BIX — extension value for BI
BDX — extension value for BD

Utility Processor State Register Format

PSRU

UNUSED	BI		BS	BD
35 27	26 18	17 16	15 9	8 0

PSRUE

UNUSED	UNUSED	BIX	BDX
35 18	17 12	11 6	5 0

PSRU — first word of utility PSR
PSRUE — second word (extension portion) of the utility PSR
BI — same as for the PSR
BS — same as for the PSR
BD — same as for the PSR
BIX — same as for the PSRE
BDX — same as for the PSRE

4.2.1. Bank Descriptor Table

The user can reload part of the active PSR from the bank descriptor table (BDT). A BDT is prepared for the user by the executive and consists of a sequence of one or more 36-bit bank descriptor words. The format of a bank descriptor word is as follows:

R	W	UNUSED	Bi	Bix	UB	LB
35	34	33	32 27	26 18	17 9	8 0

R — residency bit (interrupt is set). In this case, the BDW may contain information needed to identify nonresident code so it can be transferred to storage before returning control to the user.
W — write protect. Causes the appropriate I-bank or D-bank no-write bit to be set in the PSR.
Bi — BI or BD
Bix — BI extension or BD extension (BIX or BDX)
UB — upper boundary of program area (I-bank or D-bank)
LB — lower boundary of program area (I-bank or D-bank)

When executing an LIJ instruction, the least significant seven bits of UB are transferred to the BS field of the currently active PSR.

4.2.2. Bank Descriptor Pointer

The location and length of a bank descriptor table (BDT) is defined by the corresponding bank descriptor pointer (BDP) register. There are two BDP registers, each having the same format; the executive BDP register is at GRS address 44_8 and the user BDP register is at GRS address 45_8. The BDP register format is as follows:

t	m
35 24	23 0

m — 24-bit absolute address of bank descriptor table
t — largest valid index, 12 bits (4096 = maximum number of entries)

4.3. INTERRUPTS

The interrupt network of the 1100/40 System is extensive. It is the means of effecting real time, multiprogramming, and time-sharing operations on the system. The interrupt is a control signal generated by either a peripheral subsystem (external interrupt), an IOAU, or the control section of a CAU. Specific interrupt locations are assigned within the lower addresses of a main or extended storage module as specified by a 9-bit module select register (MSR). These interrupt locations are programmed to capture the interrupted address and enter interrupt response subroutines in the executive system. The synchronization of input/output activities and response to real time situations are accomplished through some of these interrupts.

Other interrupts are provided for certain error conditions detected within a CAU or IOAU. These may result from a programming fault such as an illegal instruction, a storage parity error, or a user program violation such as an attempt to write into a protected area of storage or a violation of guard mode. These fault interrupts are used by the executive to initiate remedial or terminating action when they are encountered.

4.4. GUARD MODE

Guard mode operation prevents user programs from executing any of the instructions listed below. These are reserved for the executive. It also permits protection of certain specified locations in main storage and control registers reserved for executive operations.

Guard mode is established by the Load Processor State Register instruction. Execution of this instruction with the appropriate PSR bit pattern is the only way that guard mode can be made operative and provides the only direct access to the PSR. Under guard mode, an attempt to perform any of the privileged instructions or functions listed below results in a guard mode fault interrupt.

- Storage limits violation when PSR bits D2 and/or D3 are set, or when a write is attempted in violation of the D13—D16 settings.

- All I/O instructions and executive system control instructions

- Disabling of I/O interrupts for more than 100 microseconds

- Attempting to write into any of the executive control registers (40_8 – 100_8 or 120_8 – 177_8) when PSR bit D2 is set.

Guard mode is disabled by the occurrence of any interrupt. This stores the contents of PSR, PSRE, PSRU, and PSRUE in GRS locations 40_8 through 43_8, clears certain bit positions of the PSR, sets D9, D7, and D6=1, and establishes executive mode operation.

5. INPUT/OUTPUT ACCESS UNIT

5.1. GENERAL

The input/output access unit (IOAU) has exclusive control over all input/output operations. An IOAU (see Figure 5—1) receives commands from the control section of either of the two command/arithmetic units (CAU) to which it is connected. Information pertaining to the channel selected and interrupts for that channel are routed back to the CAU that requested that operation.

The basic IOAU section has eight channels and may be expanded by eight-channel increments to 24 channels. Any channel can be operated in either the internally specified index (ISI) or externally specified index (ESI) mode. When operating in either the ISI or ESI mode, data chaining is provided. Base relocation registers are provided for converting the relative address in an access control word (ACW) to an absolute address. External interrupt and monitor interrupt tabling in the ESI mode are provided with a table pointer for each channel.

5.1.1. Storage Interface

The IOAU has one access path to each cabinet of main storage and dual access paths to extended storage. All channels have ESI, ISI, and interrupt tabling capabilities. Channels may be individually selected to operate in either the ESI or ISI mode. Each IOAU interfaces with all of primary storage and extended storage. The paths to the multiple access interface (MAI) and the multi-module access (MMA) units have overlapping capabilities allowing faster cycle time. The IOAU selection sequence of the multiple access interface units may be altered to allow extended storage interleaving. The sequence selection is designed to permit maintenance of individual storage units without any effect on the rest of the system.

The IOAU has the ability to logically connect an input and an output channel back to back (physical connection required) under executive control allowing storage transfers between the extended storage subsystem and main storage by means of IOAU storage interface paths.

5.1.2. Day Clock

Each IOAU includes a 36-bit day clock. The day clock is incremented once each 200 microseconds. The day clocks interrupt the appropriate CAU at 6.5536-second intervals. Each day clock can be enabled and disabled under program control; in addition, the day clocks can be manually disabled.

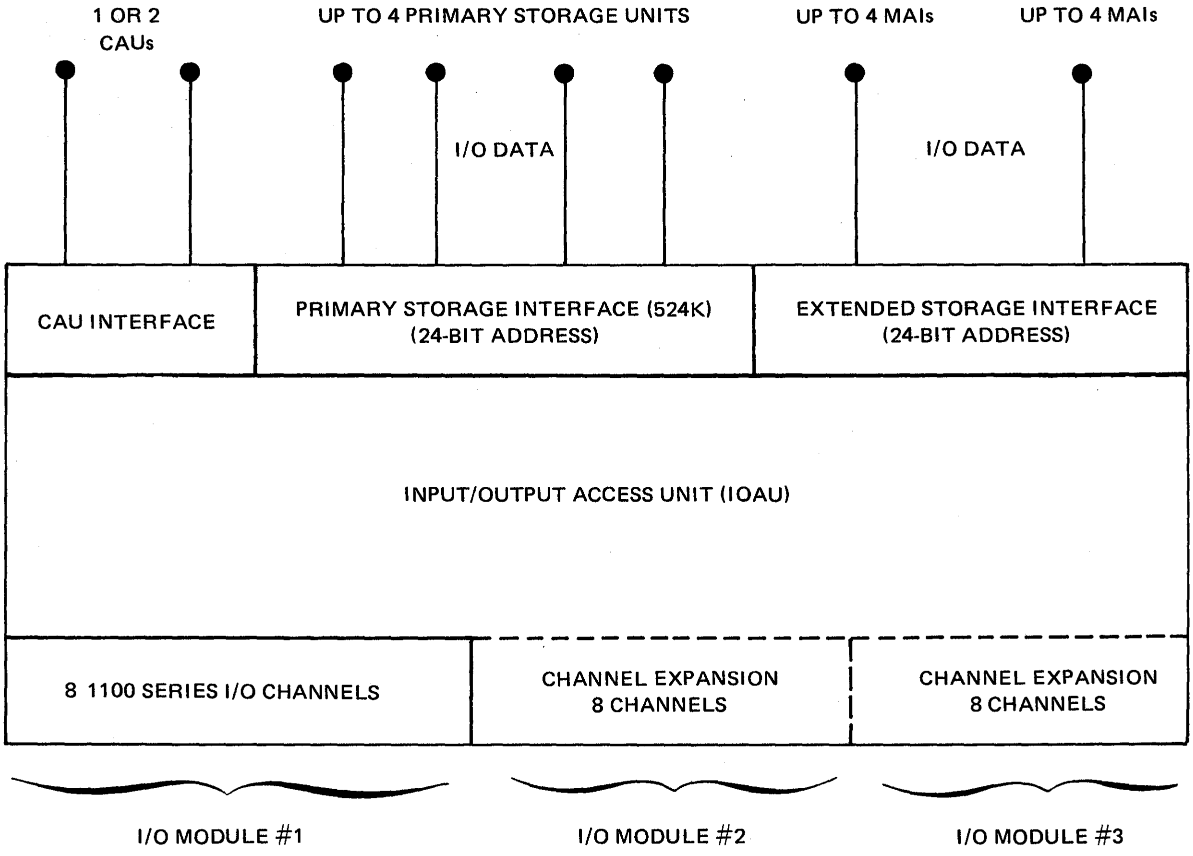


Figure 5–1. Input/Output Access Unit

5.2. INTERNALLY SPECIFIED INDEX MODE

In the internally specified index (ISI) mode, each I/O channel operates in one of three states: input, output, and function. Input and output are the data transmission states. The function state is actually an output state during which the processor sends one or more function words to the subsystem. Each function word specifies an operation to be performed by the subsystem.

The actual word-by-word transmission (regardless of transfer state) is governed by an access control word stored in an access control register. Two of these registers, one for input and one for output, are assigned to each I/O channel.

The format of the ISI access control word is as follows:

G	W WORD COUNT	V STARTING ADDRESS
35 34	33 18	17 0

V — 18 bits, the relative starting address for data transfer.
W — 16 bits, the number of words still to be transferred. It decreases by 1 each time a word is transferred.
G — 2 bits, the incrementation control for V.
= 00, increment V by 1 after each word is transferred.
= 10, decrement V by 1 after each word is transferred.
= 01 or 11, do not change V.

In initiating an input/output operation, the CAU sends an access control word to the IOAU, which is then loaded in the IOAU control register associated with a given channel. Depending on the contents of G, the I/O control section transfers subsequent words to or from successive locations in storage (increasing or decreasing addresses) or to or from a single location. After each transfer the word count, W, is decreased by one and tested for zero. A nonzero calls for transfer of the next word in the block; a zero terminates the transfer; and if the instruction calls for monitoring, the input/output monitor interrupt is set.

5.2.1. ISI Data Chaining

Data chaining is the linking of a series of access control words to provide the IOAU with the capabilities for scatter/read, gather/write operations. The ACW are sequentially replaced whenever the ISI input/output ACW count field (W) is decreased from one to zero.

Whenever an input or output word count field (W) is decreased from one to zero, a chain sequence to replace it and the associated data chain pointer word (CPW) are initiated if bit 18 of the current CPW is equal to one. The new ACW and CPW are then read from two consecutive storage addresses specified by the address field of the current CPW plus chain base register (CBR). Data chaining continues until a CPW with bit 18 equal to zero is detected. Chaining will not occur if the word count field of the ACW equals zero initially. The format of the CPW is as follows:

BASE FOR ACW V FIELD	NOT USED		ADDRESS OF NEXT ACW
35 21	20 19	18	17 0

DATA CHAIN BIT

Bits 35—21 Base value that is added to V field of ACW to form absolute address for data or function word transfer.

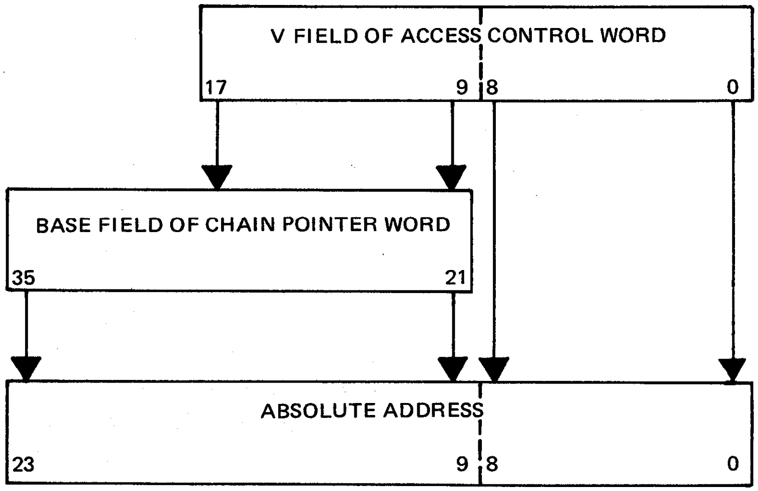
Bits 20—19 Zeros.

Bit 18 Bit 18 equal to one: specifies data chaining for all ISI input or output. Bit 18 equal to zero: specifies no chaining. Bit 18 must be zero for a function transfer.

Bits 17—0 The relative address of the next ACW for chaining. A one is added to the address for next chain pointer word. The absolute address of the next ACW is formed by adding the contents of the chain base register (CBR) to the relative address (bits 17—0) to form a 24-bit absolute address.

5.2.2. ISI Absolute Address Generation

The absolute address for an ISI data or function transfer is formed by adding the address of the V field in the access control word and the base field of the chain pointer.


V FIELD OF ACCESS CONTROL WORD
17
9
8
0
BASE FIELD OF CHAIN POINTER WORD
35
21
ABSOLUTE ADDRESS
23
9
8
0

5.2.3. ISI External Interrupts

When an IOAU receives an external interrupt signal from a subsystem, it responds as follows:

- Through the operation of the I/O priority network in the appropriate CAU, its instruction sequence is altered and the next instruction is obtained from the ISI external interrupt location.
- The status word on the input word/status word lines is transferred to a specifically reserved location in main storage as determined by the memory select register, the CAU number, and the IOAU number.
- The input acknowledge signal is transmitted to the subsystem. The subsystem turns off the external interrupt and status word signals.

5.2.4. ISI Monitor Interrupts

A monitor interrupt is initiated if the transfer was initiated by the execution of a Load Input Channel and Monitor, Load Output Channel and Monitor, or Load Function Channel and Monitor instruction after the word count field has been decremented to zero and the chain bit of the chain pointer word is zero.

When a monitor interrupt occurs, the sequence of instruction being executed is altered. The next instruction to be executed is obtained from the appropriate ISI monitor interrupt location in main storage.

5.2.5. Back-to-Back Mode

A special ISI channel back-to-back data transfer mode is provided. This special mode allows execution of back-to-back storage transfers between areas of primary and extended storage concurrently with normal I/O operation. Only one channel within the IOAU operates in this mode at any given time. The channel input and output must be connected with a back-to-back cable.

5.3. EXTERNALLY SPECIFIED INDEX MODE

The externally specified index (ESI) mode, in conjunction with data communications equipment, allows multiplexed remote communication devices to communicate with main storage over a single I/O channel on a self-controlled basis without disturbing the main program. Each such remote device communicates with its own area of main storage.

Any I/O channel can be set to ESI mode. Furthermore, by means of a patch card, an ESI channel can be set to operate in either half-word (18-bit) or quarter-word (9-bit) mode.

Because an I/O channel can be used by many devices in ESI mode, data flow must be governed by an access control word unique to the device currently in operation rather than to the channel as in ISI. These access control words are held in main storage at relative addresses assigned to the devices. As a device transfers data; it presents the relative address of its own access control word; thus, no complicated program monitoring is necessary to control data flow. The contents of the 9-bit memory select register (MSR) are used to extend the 15-bit relative address to produce a 24-bit absolute address of the ACW.

The format for the ESI access control word differs somewhat from that for ISI to enable control of half- and quarter-word transfers. The half-word access control word is as follows:

G	H	W WORD COUNT	V STARTING ADDRESS
35 34	33	32 18	17 0

The G, W, and V fields have the same meaning as in the ISI access control word except that W is reduced to 15 bits and counts half-words. There is also a one-bit H field; this field is used to indicate which half of location V is to be used, as follows:

SECOND HALF-WORD H = 1	FIRST HALF-WORD H = 0
35 18	17 0

H = 0; use first half-word of location V and switch H to 1.
H = 1; use second half-word of location V, change V address as specified by G, decrement word count W, and switch H to 0.

Quarter-word operations are similar to half-word operations except that additional programmed control is provided in terminating transmission. For this purpose the access control word includes two extra control bits. The quarter-word access control word is as follows:

G	H	C	W WORD COUNT	V STARTING ADDRESS
35 34	33 32	31 30	29 18	17 0

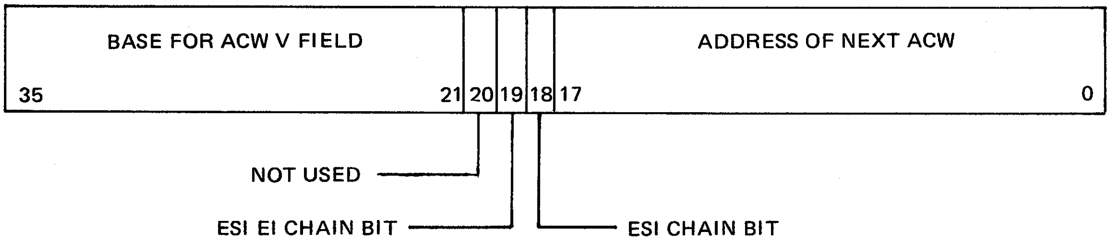
G, W, and V have the same meaning as for ISI and W is now only 12 bits long and now counts qurater-words. H indicates which quarter-word portion of V is being addressed as follows:

FIRST QUARTER-WORD H=00	SECOND QUARTER-WORD H=01	THIRD QUARTER-WORD H=10	FOURTH QUARTER-WORD H=11
35 27	26 18	17 9	8 0

C is a two-bit control field for use in output operations that prevents loss of data by generating an extra programmed monitor interrupt, if required, and a programmed end-of-transmission signal. The normal monitor interrupt occurs when W goes from 1 to 0. However, when bit 30 is set to 1, the IOAU sends a monitor interrupt to a CAU when W decreases from 2 to 1. Similarly, if bit 31 is set to 1, the IOAU generates the end-of-transmission signal as W goes from 2 to 1.

5.3.1. ESI Data Chain Pointer

Each ESI access control word (ACW) has an associated chain pointer word located in the next higher storage location. The format of the ESI chain pointer word is as follows:



Bits 35–21 Base value that is added to V field of ACW to form absolute address for data or function word transfer.

Bit 20 Zero

Bit 19 Bit 19 equal to one: specifies data chaining when an ESI external interrupt occurs. Bit 19 equal to zero: specifies no chaining.

Bit 18 Bit 18 equal to one: specifies data chaining for all ESI input or output. Bit 18 equal to zero: specifies no chaining. Bit 18 must be zero for a function transfer.

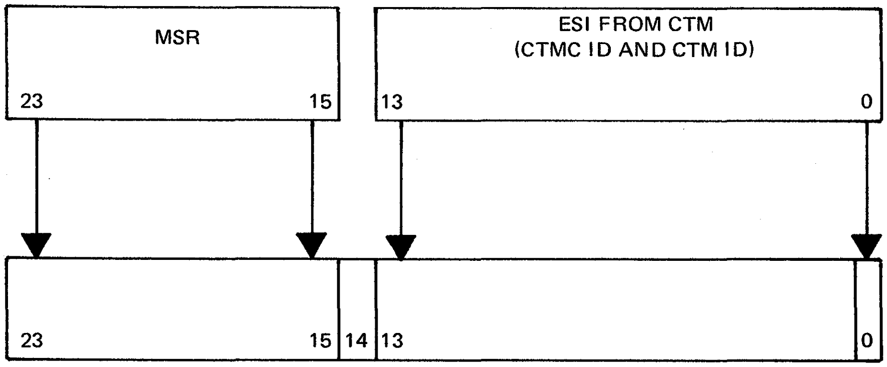
Bit 17–0 The relative address of the next ACW for chaining. A one is added to the address for next chain pointer word. The absolute address of the next ACW is formed by adding the contents of the chain base register (CBR) to the relative address (bits 17–0) to form a 24-bit absolute address.

5.3.2. ESI Absolute Address Generation

When a remote device has an input character for, or can accept an output character from, the IOAU, its ESI value is presented to the IOAU. The ESI value has the following format:

INPUT DATA	NOT USED	CTMC ID	CTM ID
35 18	17 14	13 6	5 0

After the ESI value is accepted by the IOAU, it is realigned and augmented with the contents of the memory select register to form the absolute ESI ACW address as shown below.



ABSOLUTE ESI ADDRESS

Bit 0 of the absolute address is zero for an ACW address. Bit 0 is one for the ESI data chain pointer word address.

To form the absolute address for ESI data transfers, the contents of the base field at the associated ESI data chain pointer word are added to the V field of the ESI ACW with the same alignment as shown in 5.2.2 for ISI address generation.

5.3.3. ESI External and Monitor Interrupt

Interrupts on ESI channels are hardware tabled. An interrupt tabling sequence is initiated in the IOAU when an ESI external interrupt occurs or when the word count field of the ESI ACW reaches the terminal condition and an input or output transfer with monitor was specified by the corresponding Load Output Channel and Monitor or Load Input Channel and Monitor instruction.

Tabling is accomplished using the contents of the channel ISI input access control register as an active ESI interrupt pointer. This pointer word specifies the number of words required to fill the table and the relative address in which to store the next interrupt status word. The channel ISI input chain pointer register holds an auxiliary ESI interrupt table pointer with the same format as the active interrupt table pointer.

The active and auxiliary pointers must be initially loaded by software and do not have to be restored by the program. During a tabling sequence, the 24-bit absolute address of the first of the two consecutive words stored for each table entry is formed by adding bits 17–0 of the active interrupt pointer and the contents of the chain base register (CBR). The contents of the chain base register are added to bit position 9 and above of the relative address to form an absolute address. After each tabling sequence, the word count of the active interrupt pointer is decreased by two and the address is increased by two.

	WORD COUNT (Must be nonzero and an even number)	RELATIVE ADDRESS OF NEXT TABLE ENTRY
35 34	33 18	17 0

NOT USED
(Must be zeros)

ESI INTERRUPT POINTER

When the word count field of the active interrupt pointer is decreased to zero, the contents of the auxiliary interrupt pointer are transferred to the active interrupt pointer location (ISI input ACW register); and an ESI table full interrupt to address 226_8 plus MSR is initiated.

The program has the option of being notified of ESI channel tabling activity either immediately upon occurrence of the activity, or by having the channel retain the fact that tabling occurred by means of the table activity designator and then interrogating this designator.

The contents of the auxiliary interrupt pointer is not disturbed by the hardware. The software has the option of allowing interrupt tabling to continue in the table or reloading the auxiliary interrupt pointer, thereby chaining the interrupt tables.

Software controls process interrupts in the table ensuring that processing is ahead of tabling. The format of the tabled interrupt status word pair is as follows:

	EI STATUS	NOT USED	UNSHIFTED ESI
35	34 18	17 14	13 0

First Word

Bit 35 Set in external interrupt status word. Cleared for monitor interrupt.

Bits 34–18 Status word for external interrupt. Zeros for monitor interrupt.

Bits 17–14 Not used.

Bits 13–0 ESI.

Second Word

Is the input or output data transfer ACW for the ESI that generated the external interrupt (see 5.3 for format). For input or output monitor, the second word is not written into storage.

5.3.4. ESI Function Word Transfer

When the Load Function in Channel or Load Function in Channel and Monitor instruction is executed, an output access control word is transferred from the location specified by the instruction to the output access control register associated with the specified output channel. When the instruction is executed, one function word is transferred from the storage location specified by the output access control word. It is transmitted by means of the output word/function word lines of the associated channel to the subsystem.

The contents of the base field of the channel output pointer register are added to the V field of the function ACW to form the absolute address.

5.3.5. ESI Buffer Termination and ESI Data Chaining

Whenever the word count field of an ESI input or output data ACW reaches the terminal condition, a sequence to replace it and the associated data CP word is initiated, if bit 18 of the current chain pointer word is a one. Whenever an ESI EI occurs, a sequence to replace the ACW and the associated data CP word are initiated if bit 19 of the current CP word is equal to one. The new ACW and chain pointer word is read from the storage address and the address plus one specified by the address field of the current data chain pointer word plus the chain base register.

ESI data chaining continues until a chain pointer word with a zero for bit 18 is encountered.

6. STORAGE

6.1. GENERAL

The SPERRY UNIVAC 1100/40 Systems incorporate a two-level hierarchy of directly addressable, executable storage. The first level, called primary storage, consists of high speed nondestructive readout semiconductor storage. The second level, called extended storage, consists of moderate cost semiconductor storage.

Design of storage in this manner not only allows more storage on the system, but permits a choice of storage media according to particular needs. For example, a frequently used computer-bound function could reside in high speed primary storage, while the less often used contingency routines associated with it would be in extended storage. Within the system, this two level storage hierarchy is treated as a set of system components in the same manner as peripheral devices, allowing efficiencies not before available in most processor systems.

Among the featured characteristics of the storage hierarchy are:

- independently accessible modules;
- continuous addressing structure;
- access priority structure in case of conflicts;
- parity checking on data, and write/read controls;
- interrupt generation in case of address or data parity error;
- ease of storage expansion; and
- partial word capability for read and write operations.

6.2. PRIMARY STORAGE

Primary storage is composed of fast access nondestructive readout (NDRO) semiconductor storage modules and built-in multi-module access (MMA) units. Among its features are:

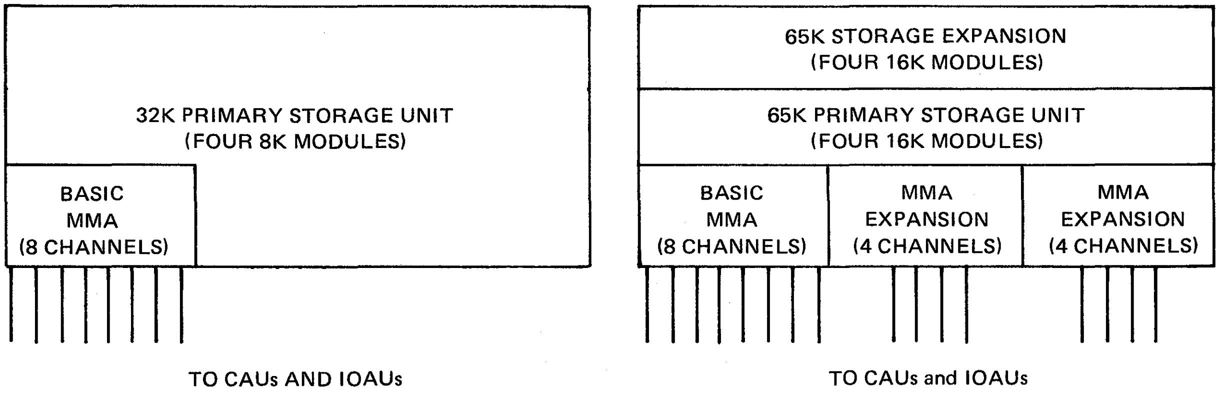
- nominal 280-nanosecond read and 380-nanosecond write cycles;
- 16,384 (16K)-word modularity for simultaneous access (except for minimum 1x1 system);
- parity checking on addresses, data, and write/read controls;

- access through the MMAs by up to four command/arithmetic units (CAUs) and four input/output access units (IOAUs);
- expandability in 65K-word increments up to primary storage capacity of 524K-words;
- interleaved access to boost performance and reduce conflicts (odd-even addressing to two adjacent 16K modules);
- access conflicts resolved on 16K boundaries; and
- partitionable in 65K-word increments.

6.2.1. Primary Storage Unit (PSU)

A PSU (see Figure 6–1) consists of a minimum of 32K words of storage, MMA, power supplies, and maintenance panel. Each word consists of 36 data bits, two parity bits (one bit per half-word), and two spare bits at non-addressable levels. Four 8K modules constitute the minimum storage unit. Or, the storage unit may consists of four 16K modules, expandable in one increment by the addition of four 16K modules for a total capacity of 131,072 (131K) words per storage unit. A total of four 131K units provide a maximum primary storage of 524K words in a system.

A basic 32K or 65K primary storage unit is capable of simultaneously servicing four requests, one per 8K or 16K module, while a fully expanded primary storage unit can service up to eight simultaneous requests.



a. 8K Module Primary Storage Unit

b. 16K Module Primary Storage Unit

Figure 6–1. Primary Storage Unit

6.2.2. Multi-Module Access Unit (MMA)

The MMA unit is physically contained in the primary storage unit cabinet and is functionally located between the primary storage unit and the CAUs and IOAUs. The MMA furnishes eight priority-ordered connection paths to each of the storage modules in the primary storage unit. The number of paths to the MMA may be increased to 12 or 16 by the use of MMA expansion features.

Should an access conflict occur among requestors, the MMA grants primary storage access to the processor having the highest priority, then the next, and so on. Communications between a requestor and a single storage module can, therefore, be asynchronous. If the storage module is busy servicing one requestor, a passive wait cycle occurs in requestors of lower priority referencing the same module. Delays in honoring I/O transfers are eliminated as the IOAUs are attached to the higher priority paths of the MMA.

6.3. EXTENDED STORAGE SUBSYSTEM

The extended storage subsystem is composed of moderate cost semiconductor storage modules and associated multiple access interfaces (MAIs). Among its features are:

- 800 nanosecond read/write cycle;
- 131K-word modularity;
- parity checking on addresses, data, and write/read controls;
- error checking and correction;
- access through the MAIs by up to four CAUs, four IOAUs, and one maintenance controller (must have access to at least 131K of extended storage);
- expandability in 131K-word increments up to a maximum of 1,048K words;
- capability of interleaved operation to boost performance and reduce conflicts (interleaves of 1 or 2 may be selected and changed at the site); and
- partitionable in 131K increments.

6.3.1. Extended Storage Unit (ESU)

Each ESU consists of 131K words of 800 nanoseconds semiconductor storage, power supplies, and maintenance panel. Each word consists of 36 data bits, two parity bits (one bit per half-word), and seven error correcting code bits.

6.3.2. Multiple Access Interface (MAI)

The MAI, operating in the same manner as the integral MMA on primary storage, interfaces with 131K of extended storage and up to four CAUs and four IOAUs. An MAI expansion may be added to the MAI, providing identical interfaces for a second extended storage unit. The MAI expansion, functionally a second MAI, shares the same cabinet and power supplies with the MAI to which it is added.

6.4. PARITY

Parity is checked on addresses presented to MMAs, MAIs, PSUs, and ESUs prior to performing the operation requested. In this way, malfunctions may be isolated, identifying the faulty component. During all read and write operations, data parity is checked at these same levels, providing the highest degree of system integrity. Upon detection of any parity error, an interrupt is generated; the status word associated with the interrupt indicates the error type and point at which the error occurred.

For each word written in extended storage, a 7-bit error correcting code is generated from the write data (36 data bits and two parity bits) and the resultant 45-bit word stored. If during a read or partial write, a single bit error is detected in the stored data, the error correcting code is used to correct the data. If multiple errors are detected in the stored data, the processor is notified with a data parity error interrupt signal.

6.5. STORAGE PROTECTION

To prevent inadvertent program reference to out of range addresses, the 1100/40 System includes a hardware storage protection feature. The controlling element in this feature is the storage limits register (SLR). Two SLRs are provided; one associated with PSR (SLR), and one associated with PSRU (SLRU). The SLR format is:

INSTRUCTION AREA		DATA AREA	
I-UPPER BOUNDARY	I-LOWER BOUNDARY	D-UPPER BOUNDARY	D-LOWER BOUNDARY
35 27	26 18	17 9	8 0

The storage limits registers (SLR and SLRU) can be loaded by the executive system to establish allowable operating areas for the program currently in execution. These areas are termed the program instruction (I) and data (D) areas. Before control is given to a particular program, the executive system loads the SLRs with the appropriate instruction and data boundaries.

Before each main storage reference, the appropriate CAU performs a limits check by comparing the relative address against the limits of the storage limits registers. An out of limits address generates a guard mode interrupt, thereby allowing the executive system to regain control and take appropriate action.

The executive system establishes a storage protection mode for the user program (see 6.5.1) by means of control fields in the processor state register (PSR). Normally, the executive itself operates in open mode; that is, the executive can reference any location in main storage, and storage limits are used only in conjunction with D18 (auto-toggle).

6.5.1. User Program Mode (Guard Mode)

In the user program mode, read, write, and jump storage protection is in effect. Therefore, user programs are limited to those areas assigned by the executive. If the user program reads, writes, or jumps to an out-of-limits address, an interrupt returns control to the executive for remedial action.

Read/jump protection allows the executive system to stop the program at the point of error, terminate it, and provide diagnostic information to the programmer thereby minimizing lost time and smoothing the checkout process.

6.6. RELATIVE ADDRESSING

Relative addressing is a feature of great significance in multiprogramming, time-sharing, and real time operation; it allows storage assignments for one program (the one going into execution) to be changed dynamically by the executive to provide continuous storage for operation of another program, and it permits programs to dynamically request additional main storage according to processing needs. An additional advantage is that systems programs stored in auxiliary mass storage may be brought in for operation in any available area without complicated relocation algorithms.

The full direct addressing capabilities of the 1100/40 System provides for the execution of instructions, the reading or writing of operands, and I/O data transfers throughout the full range of the system.

The 1100/40 System addressing mode provides an 18-bit relative addressing range of 262K words with any given PSR setting. The user may switch from two hardware PSR settings. Programs may be relocated on 512-word block boundaries.

6.7. CHARACTER ADDRESSING

The 1100/40 System is provided with extended character addressing capabilities and with the ability to manipulate character addresses in essentially the same manner as full-word addresses. There are two character addressing modes:

- The 1100/40 System character instruction subsets:
  - Byte instructions
  - Byte/binary conversions
  - Decimal arithmetic instructions
- Instructions specifying:
  - Instruction f-field values less than 70_8 (except 07_8, 33_8, 37_8)
  - Instruction j-field values of 4_8 through 7_8 defined by addressing one of the four J registers located in R registers R6 through R9.
  - Bit D4 in the processor state register specifying character indexing mode

7. AUXILIARY STORAGE AND PERIPHERAL SUBSYSTEMS

7.1. AVAILABLE AUXILIARY STORAGE AND PERIPHERAL EQUIPMENT

Auxiliary storage and peripheral subsystems are attached to the SPERRY UNIVAC 1100/40 System through general purpose input/output (I/O) channels, which have no restriction as to the manner in which peripheral subsystems may be attached. The governing factor for peripheral attachment is the transfer rate of the devices in the subsystem. Since the channels are numbered in order of priority, real-time operations with very high transfer rates should be attached to the lower numbered channels which have the higher priority.

The SPERRY UNIVAC 1100/40 Auxiliary Storage and Peripheral Subsystems are:

- Mass Storage

  SPERRY UNIVAC 8405 Disc Subsystem
  SPERRY UNIVAC 8430 Disc Subsystem
  SPERRY UNIVAC 8433 Disc Subsystem
  SPERRY UNIVAC 8425 Disc Subsystem

- High Performance Drum

  FH–432/FH–1782 Magnetic Drum Subsystem

- Magnetic Tape

  UNISERVO 12 Magnetic Tape Subsystem
  UNISERVO 16 Magnetic Tape Subsystem
  UNISERVO 20 Magnetic Tape Subsystem

- Byte Interface Paper Peripheral Subsystems

  SPERRY UNIVAC 0770 Printer
  SPERRY UNIVAC 0716 Card Reader
  SPERRY UNIVAC 0604 Card Punch
  SPERRY UNIVAC 0920 Paper Tape via the C/SP

- SPERRY UNIVAC Multi-Subsystem Adapter (MSA)

- SPERRY UNIVAC Communications/Symbiont Processor (C/SP)

Auxiliary storage and peripheral subsystems used on earlier model SPERRY UNIVAC 1100 Series Systems can be configured, but Sperry Univac will not develop any new software for these destandardized subsystems.

7.2. SPERRY UNIVAC DISC SUBSYSTEMS

Sperry Univac offers a variety of disc storage subsystems for use on the **1100/40** Systems. Basic subsystems can include:

SPERRY UNIVAC 8405 Disc
SPERRY UNIVAC 8430 Disc
SPERRY UNIVAC 8433 Disc
SPERRY UNIVAC 8425 Disc

The advantages achieved by implementing disc subsystems include:

- substantially increased throughput performance

- provision for incremental growth

- expanded potential for online processing

- enhanced capabilities for real time and multiprogramming

- intermix of 8405 (fast access) and 8430 or 8433 (large capacity) on same subsystem

- error correction code

- command retry

Disc subsystems provide the **1100/40** System with an expandable, fixed or removable direct access, external storage medium.

Data is transferred between the CPU and the disc subsystems one word at a time. The SPERRY UNIVAC control units for the 8405, 8430, 8433, and 8425 Disc Subsystems provide for connection to the word channels of the 1100/20 System. They also provide for data translation, function chaining, and command chaining.

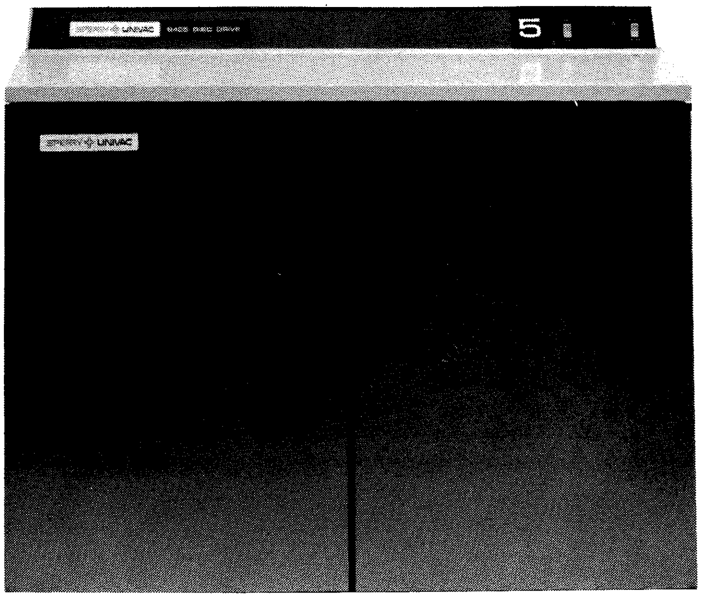
The disc subsystems offer many processing advantages, especially in applications where rapid file processing and sort/merge routines are prevalent. The removability characteristics of the disc packs permit virtually unlimited offline storage and easy interchange of information without conversion to other media.

The disc subsystems also provide for simultaneous dual access operation and prepositioning of access arms where applicable. This implies:

- Simultaneous read/read, read/write, write/read, write/write concurrent with positioning functions.

- Alternate data and command paths available to any component of the system.

7.2.1. SPERRY UNIVAC 8405 Disc Subsystem



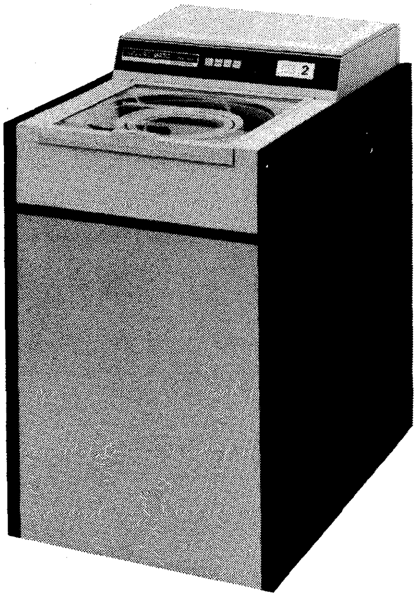
The SPERRY UNIVAC 8405 Fixed Head Disc Subsystem offers a fast access storage capacity of up to 24.7 or 49.5 million bytes, or up to 5.5 or 11.0 million 36-bit words of data online.

The 1100/40 Systems are capable of retrieving specific records without a sequential search through the record files. This retrieval permits direct access to active files and gives more efficient throughput for the processor. Random inquiries also can be made while records are being processed, or the records can be supplied sequentially for processing. Fixed heads are used in the 8405 disc storage unit. Each disc surface has eight read/write head pads, each pad containing nine read/write elements (or channels). This arrangement provides 72 read/write channels per disc surface. Each disc surface has 72 tracks, and each track is addressed by a fixed read/write head. Each disc storage unit contains 6 or 12 recording surfaces; 384 (plus 48 spares) or 768 (plus 96 spares) read/write heads are mounted in fixed positions for these recording surfaces. Because the heads are fixed and switched electronically, access time is reduced to an average of 8.3 milliseconds. The disc pack is non-removable. The 8405 disc storage unit may be mixed with 8430 and 8433 disc storage units on the same control unit.

CHARACTERISTICS

	8405–00	8405–04
NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	1–8	1–8
NUMBER OF DISC DRIVES PER STORAGE UNIT	1	1
NUMBER OF R/W HEAD ACCESSOR MECHANISMS	1 (fixed head)	1 (fixed head)
NUMBER OF R/W HEAD PADS (9 R/W ELEMENTS EACH)	96	48
NUMBER OF TRACKS PER DISC SURFACE	72	72
NUMBER OF RECORDING SURFACES PER DISC UNIT	12	6
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	64 (plus 8 spares)	64 (plus 8 spares)
NUMBER OF TRACKS PER DISC UNIT	768 (plus 96 spares)	384 (plus 48 spares)
NUMBER OF 36-BIT WORDS PER RECORD	112	112
MAXIMUM NUMBER OF RECORDS PER TRACK	16	16
CAPACITY 36-BIT WORDS PER DISC UNIT	1,376,256	688,128
AVERAGE LATENCY TIME	8.3 milliseconds	8.3 milliseconds
DISC DRIVE SPEED	3,600 rpm	3,600 rpm
STORAGE TRANSFER RATE	622,000 bytes per second 138,222 36-bit words per second	622,000 bytes per second 138,222 36-bit words per second
DUAL ACCESS	Feature available	Feature available

7.2.2. SPERRY UNIVAC 8430 Disc Subsystem



The SPERRY UNIVAC 8430 Disc Subsystem offers a large storage capacity of up to 1600 million bytes or up to 275 million 36-bit words of data online. A single disc pack provides for 77.3 million bytes or 17.1 million 36-bit words using 112-word records. Maximum capacity using free format, one record per track, is 100 million bytes or 22.2 million 36-bit words.

Each disc pack contains 11 discs. Nineteen read/write heads are mounted on a single accessor mechanism which moves the 19 heads in unison between the periphery and the central area of the disc. The accessor mechanism can assume one of 411 tracks across the disc surface. The simultaneous head movement creates 411 addressable data recording cylinders in the disc pack. Each cylinder contains nineteen tracks, numbered 0 through 18. The addressing of an individual track in the pack is by track number (000–410) and by read/write head number (0–18).

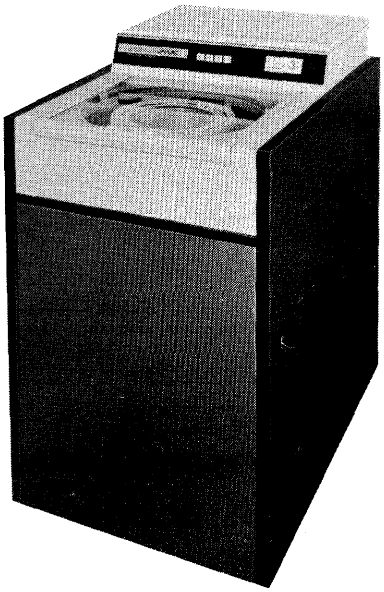
Each disc pack contains 11 discs. Nineteen read/write heads are mounted on a single accessor mechanism which moves the 19 heads in unison between the periphery and the central area of the disc. The accessor mechanism can assume one of 411 tracks across the disc surface. The simultaneous head movement creates 404 plus 7 spare addressable data recording cylinders in the disc pack. Each cylinder contains nineteen tracks, numbered 0 through 18. The addressing of an individual track in the pack is by track number (000–410) and by read/write head number (0–18).

Access to different tracks within a cylinder is faster than access to tracks in different cylinders since changing tracks requires only electronic switching whereas accessing a different cylinder requires physical movement of the accessor mechanism. There are 7809 (411 x 19) tracks, including 133 spare tracks, in a disc pack assembly. The 8430 disc storage unit may be mixed with 8405 and/or 8433 disc storage units on the same control unit.

CHARACTERISTICS

NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	1–16
NUMBER OF DISC PACKS PER STORAGE UNIT	1
NUMBER OF R/W HEAD ACCESSOR MECHANISMS	1
NUMBER OF R/W HEADS PER DISC PACK	19 (one per surface)
NUMBER OF TRACKS PER DISC SURFACE	411
NUMBER OF RECORDING SURFACES PER DISC PACK	19
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	404 (plus 7 spares)
NUMBER OF ADDRESSABLE TRACKS PER DISC PACK	7676 (plus 133 spares)
NUMBER OF WORDS PER RECORD	112
NUMBER OF 112 WORD RECORDS PER TRACK	20
CAPACITY PER DISC PACK USING 112 WORD RECORDS	17,194,240 36-bit words 77,374,084 bytes
MAXIMUM CAPACITY PER DISC PACK USING FREE FORMAT–ONE RECORD PER TRACK	22,226,284 36-bit words 100,018,280 bytes
MINIMUM ACCESS TIME	7 milliseconds
AVERAGE ACCESS TIME	27 milliseconds
MAXIMUM ACCESS TIME	50 milliseconds
DISC PACK SPEED	3600 rpm
DATA TRANSFER RATE	179,111 36-bit words per second 806,000 bytes per second
DUAL ACCESS	Feature available

7.2.3. SPERRY UNIVAC 8433 Disc Subsystem



The SPERRY UNIVAC 8433 Disc Subsystem offers a large storage capacity of up to 3200 million bytes or up to 550 million 36-bit words of data online. A single disc pack provides for 154.7 million bytes or 34.3 million 36-bit words using 112-word records. Maximum capacity using free format, one record per track, is 200 million bytes or 44.4 million 36-bit words.

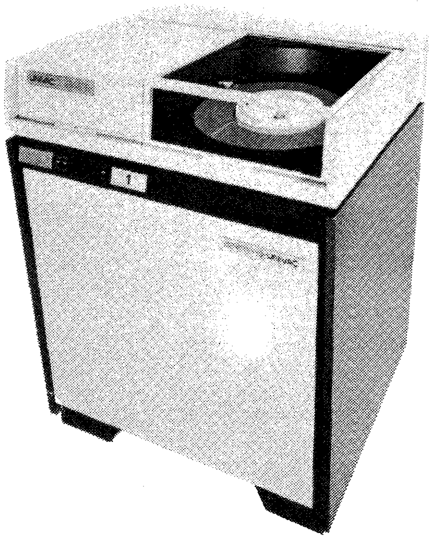
Each disc pack contains 11 discs. Nineteen read/write heads are mounted on a single accessor mechanism which moves the 19 heads in unison between the periphery and the central area of the disc. The accessor mechanism can assume one of 815 tracks across the disc surface. The simultaneous head movement creates 808 plus 7 spare addressable data recording cylinders in the disc pack. Each cylinder contains nineteen tracks numbered 0 through 18. The addressing of an individual track in the pack is by track number (000–814) and by read/write head number (0–18).

Access to different tracks within a cylinder is faster than access to tracks in different cylinders since changing tracks requires only electronic switching whereas accessing a different cylinder requires physical movement of the accessor mechanism. There are 15,485 (815 x 19) tracks, including 133 spare tracks, in a disc pack assembly. The 8433 disc storage unit may be mixed with 8405 and/or 8430 disc storage units on the same control unit.

CHARACTERISTICS

NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	1–16
NUMBER OF DISC PACKS PER STORAGE UNIT	1
NUMBER OF R/W HEAD ACCESSOR MECHANISMS	1
NUMBER OF R/W HEADS PER DISC PACK	19 (one per surface)
NUMBER OF TRACKS PER DISC SURFACE	815
NUMBER OF RECORDING SURFACES PER DISC PACK	19
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	808 (plus 7 spares)
NUMBER OF ADDRESSABLE TRACKS PER DISC PACK	15,352 (plus 133 spares)
NUMBER OF WORDS PER RECORD	112
NUMBER OF 112 WORD RECORDS PER TRACK	20
CAPACITY PER DISC PACK USING 112 WORD RECORDS	34,388,480 36-bit words 154,748,160 bytes
MAXIMUM CAPACITY PER DISC PACK USING FREE FORMAT—ONE RECORD PER TRACK	44,452,555 36-bit words 200,036,500 bytes
MINIMUM ACCESS TIME	10 milliseconds
AVERAGE ACCESS TIME	30 milliseconds
MAXIMUM ACCESS TIME	55 milliseconds
DISC PACK SPEED	3600 rpm
DATA TRANSFER RATE	179,111 36-bit words per second 806,000 bytes per second
DUAL ACCESS	Feature available

7.2.4. SPERRY UNIVAC 8425 Disc Subsystem



The SPERRY UNIVAC 8425 Disc Subsystem offers a large storage capacity of up to 466 million bytes or up to 87.3 million 36-bit words of data online. A single disc pack provides for up to 49 million bytes or 10.9 million 36-bit words. Maximum capacity using free format, one record per track, is 58 million bytes.

Each disc pack contains 11 discs. Twenty read/write heads are mounted on a single accessor mechanism which moves the 20 heads in unison between the periphery and the central area of the disc. The accessor mechanism can assume one of 406 tracks across the disc surface. The simultaneous head movement creates 400 plus 6 spares addressable data recording cylinders in the disc pack. Each cylinder contains twenty tracks, numbered 0 through 19. The addressing of an individual track in the pack is by track number (000—405) and by read/write head number (0—19).

Access to different tracks within a cylinder is faster than access to tracks in different cylinders since changing tracks requires only electronic switching whereas accessing a different cylinder requires physical movement of the accessor mechanism. There are 8120 (406 x 20) tracks, including 120 spare tracks, in a disc pack assembly.

CHARACTERISTICS	
NUMBER OF DISC STORAGE UNITS PER CONTROL UNIT	2–8
NUMBER OF DISC PACKS PER STORAGE UNIT	1
NUMBER OF R/W ACCESSOR MECHANISMS	1
NUMBER OF R/W HEADS PER DISC PACK	20 (one per surface)
NUMBER OF TRACKS PER DISC SURFACE	406
NUMBER OF RECORDING SURFACES PER DISC PACK	20
NUMBER OF ADDRESSABLE TRACKS PER SURFACE	400 (plus 6 spares)
NUMBER OF ADDRESSABLE TRACKS PER DISC PACK	8000 (plus 120 spares)
NUMBER OF WORDS PER RECORD	112
NUMBER OF 112 WORD RECORDS PER TRACK	12
CAPACITY PER DISC PACK	10,913,280 36-bit words 49,109,760 bytes
MINIMUM ACCESS TIME	7.5 milliseconds
AVERAGE ACCESS TIME	29 milliseconds
MAXIMUM ACCESS TIME	55 milliseconds
DISC PACK SPEED	2400 rpm
DATA TRANSFER RATE	69,333 words per second 312,000 bytes per second

7.3. FLYING HEAD DRUMS

The flying head (FH) series of high speed large capacity magnetic drum storage units, offered by Sperry Univac, provide modular auxiliary storage essential for the operation of large and complex systems. These units vary from the high speed FH–432 Magnetic Drum (with an average access time of 4.3 milliseconds) to the large capacity (2 million 36-bit words) FH–1782 Magnetic Drum which provides extensive fast access storage that can be used for large data files that have to be referenced frequently. Flying head magnetic drum subsystems have an individual read/write head for each track.

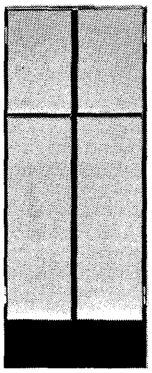
7.3.1. FH–432/1782 Magnetic Drum Subsystem

A valuable characteristic of SPERRY UNIVAC 1100/40 Drum Subsystem is the ability to associate, in the same subsystem, the high speed FH–432 Magnetic Drum with the fast high capacity FH–1782 Magnetic Drum. Any combination of eight drums may be mixed on a subsystem.

This subsystem arrangement is of significant importance in the 1100/40 System storage configuration. An efficient blend can be made of high speed storage (for rapidly required software, program segments, tables, and indices) with greater access time but large capacity storage (for less frequently used program segments, data files, and message assembly/disassembly areas). A judicious mix of speed, capacity, and economy can be planned and the mix can readily be altered as requirements change. Character transfer rates are identical for the FH–432 and FH–1782 Magnetic Drums. The only functional difference is the difference in access time and in capacity.

This subsystem is available in both single- and dual-channel versions to provide a hierarchy of auxiliary storage for the CPU. The dual-channel version includes two electrically and logically independent control units, each on a different I/O channel. This enables simultaneous operation of any two drums in the subsystem.

7.3.1.1. FH–432 Magnetic Drum



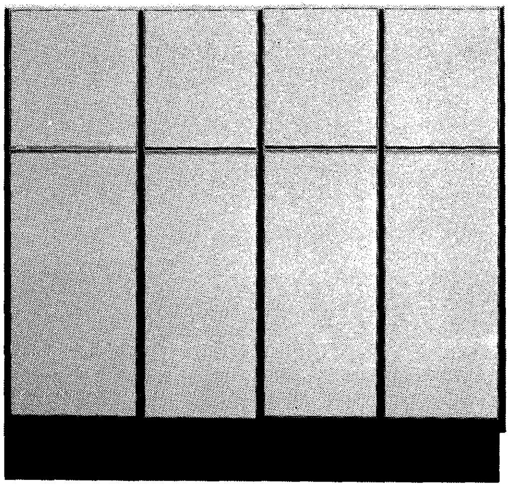
The FH–432 Magnetic Drum contains 262,144 36-bit words of storage. To augment the systems, cabinets may be added, each containing one drum with a storage capacity of 262,144 36-bit words. Of the 486 tracks on each drum, 384 are used for data; the remaining tracks are used for spares, parity, and timing functions. There are 2,048 words of data per three tracks. Reading and writing are 3-bit parallel operations on all three tracks of a band simultaneously. Thus the maximum transfer rate is 240,000 words or 1,440,000 alphanumeric characters per second.

Up to eight FH–432 Magnetic Drums may be accommodated in a single subsystem, affording a maximum subsystem capacity of 2,097,152 words or 12,582,912 alphanumeric characters.

FH–432 Magnetic Drums may be intermixed with FH–1782 Magnetic Drums in the same subsystem to provide a power blend of ultrahigh speed and large capacity storage.

CHARACTERISTICS	
STORAGE CAPACITY	262,144 computer words of 36 data bits plus parity bits, or 1,572,864 alphanumeric characters per drum
AVERAGE ACCESS TIME	4.3 milliseconds
DRUM SPEED	7,200 revolutions per minute
NUMBER OF READ/WRITE HEADS FOR DATA	384 – one per track
CHARACTER TRANSFER RATES	1,440,000; 720,000; 360,000; 180,000; 90,000
WORD TRANSFER RATES	240,000; 120,000; 60,000; 30,000; 15,000
I/O CHANNELS REQUIRED	1 or 2 per subsystem
NUMBER OF DRUMS PER SUBSYSTEM	1 to 8 (12,582,912 characters maximum)

7.3.1.2. FH–1782 Magnetic Drum



The FH–1782 Magnetic Drum is similar to the FH–432 Magnetic Drum except that average access time is four times greater and the storage capacity is eight times greater; this increase is achieved partly by an increase in the number of data tracks to 1,536 and partly by an increase in the recording density. Each track has its own read/write head, and average access time is 17 milliseconds.

A single FH–1782 Magnetic Drum stores 2,097,152 words, equivalent to 12,582,912 alphanumeric characters. Up to eight FH–1782 Magnetic Drums can be accommodated in a single subsystem giving a subsystem capacity of 100,663,296 characters.

The data transfer rate of the FH–1782 Magnetic Drum is equal to that of the FH–432 Magnetic Drum; this arrangement enables FH–1782 Magnetic Drums to be associated with FH–432 Magnetic Drums, in the same subsystem.

CHARACTERISTICS	
STORAGE CAPACITY	2,097,152 computer words of 36 data bits plus parity bits, or 12,582,912 alphanumeric characters per drum
AVERAGE ACCESS TIME	17 milliseconds
DRUM SPEED	1,800 revolutions per minute
NUMBER OF READ/WRITE HEADS FOR DATA	1,890 (35 blocks with 54 heads per block)
CHARACTER TRANSFER RATES	1,440,000; 720,000; 360,000; 180,000; 90,000
WORD TRANSFER RATES	240,000; 120,000; 60,000; 30,000; 15,000
I/O CHANNELS REQUIRED	1 or 2 per subsystem
NUMBER OF DRUMS PER SUBSYSTEM	1 to 8 (100,663,296 characters maximum)

7.4. UNISERVO MAGNETIC TAPE SUBSYSTEMS

Three SPERRY UNIVAC Magnetic Tape Subsystems are available with the 1100/40 Systems. These subsystems may include:

UNISERVO 12 Magnetic Tape Units
UNISERVO 16 Magnetic Tape Units
UNISERVO 20 Magnetic Tape Units

The advantages provided by these magnetic tape subsystems include:

- wide range of performance

- intermix of units

- simultaneous dual access

- cartridge capability

- PE, NRZI — 7 and 9 track — variety of densities

Two basic methods of operation are available. These methods of operation are:

- Nonsimultaneous (single channel operation) — In this method of operation, one or more tape units are connected to a single I/O channel through the appropriate control unit. Only one function, on any one of the tape units, may be active at any single instant.

- Simultaneous Operation (two channel operation) — In this method of operation, two or more tape units are connected to two I/O channels through two control units.

A UNISERVO 12 Magnetic Tape Subsystem (partial-simultaneous subsystem) provides for read/read, read/write, write/read on any two individual UNISERVO 12 Magnetic Tape Units. All other tape units may be rewound concurrently. Write/write simultaneity operation is available only through separate master units. Appropriate simultaneous features must be added to the UNISERVO 12 Master Tape Units but are not software supported.

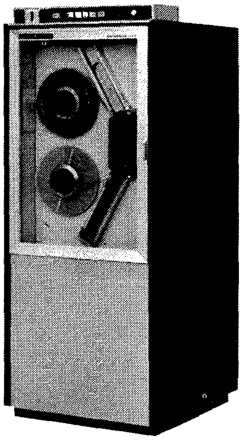
UNISERVO 16 Magnetic Tape Subsystems and UNISERVO 20 Magnetic Tape Subsystems (fully simultaneous dual access subsystems) provide for read/read, read/write, write/read and write/write operation on any two individual tape units. All other tape units may be rewound concurrently. Dual access provides two independent access paths to each UNISERVO 16 or UNISERVO 20 Magnetic Tape Unit. Tape units in these configurations must contain the appropriate dual access features. In addition to doubling the performance of the subsystem; simultaneous, dual access operation, includes complete power redundancy by virtue of individual power supplies per control unit. UNISERVO 12 Magnetic Tape Subsystems are not permitted in this configuration.

"On the fly" single-track mode error correction is standard for phase tapes. On 9-track NRZI tapes, single-track read error correction is provided by a second attempt of an operation after error detection and repositioning. This provides the ability to correct tape errors in either the forward or backward direction. This simplifies the error correction programming routines and assists in the recovery of unusual error conditions which otherwise would results in a nonrecoverable error. A programmable low gain read assists in the reading of tape records containing high noise levels.

Magnetic tape subsystems may consist of 16 tape units with the appropriate control units. Subsystems are available for both 7- and 9-track operation. The 7- and 9-track options permit data recorded in industry compatible form to be handled and records upgraded in line with the ASCII code and packed-decimal formats at the same time.

The control unit includes an integral MSA capability, and provides for optional data translators (Fieldata code from/to a 64-character subset of ASCII and Fieldata code from/to a 64-character subset of EBCDIC) and shared peripheral interface (SPI). The control unit can also accommodate UNISERVO 12 and 16 Magnetic Tape Units and thus provide for optional 7- and 9-track NRZI tape operation.

7.4.1. UNISERVO 12 Magnetic Tape Subsystem



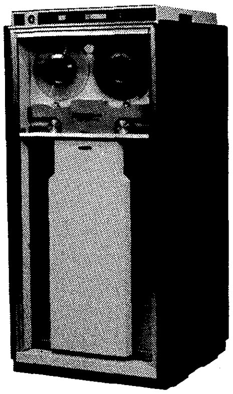
The UNISERVO 12 Magnetic Tape Subsystem is a low-cost medium performance subsystem with 7- or 9-track, 200, 556, or 800 bpi NRZI and 1600 bpi phase encoding as the available tape formats. One master tape unit, with a power supply and control circuits, controls up to three slave units. Up to 16 tape units are synchronously controlled by a UNISERVO 12/16 Control Unit.

This subsystem offers a peak transfer rate of 68,000 frames per second in phase encoding recording. The 7- or 9-track NRZI formats with a peak transfer rate of 34,000 frames per second also can be incorporated. Tape data validity checking facilities include read check while writing, longitudinal redundancy check, vertical parity check (9-track phase tapes) and cyclic redundancy check (diagonal, 9-track NRZI tapes).

CHARACTERISTICS

RECORDING DENSITY (PE)	1600 bpi
RECORDING DENSITY (NRZI)	200, 556, or 800 bpi
TRANSFER RATE (PE)	68,320 frames per second
TRANSFER RATE (NRZI)	8,540; 23,741; or 34,160 frames per second
TAPE SPEED	42.7 inches per second
TAPE WIDTH	0.5 inch
TAPE LENGTH (MAX.)	2,400 feet
BLOCK LENGTH	Variable
INTERBLOCK GAP	0.75 inch (7-track) 0.6 inch (9-track)
INTERBLOCK GAP TIME (7-TRACK)	17.6 milliseconds (nonstop) 23.6 milliseconds (start/stop)
INTERBLOCK GAP TIME (9-TRACK)	14.1 milliseconds (nonstop) 20.1 milliseconds (start/stop)
REVERSAL TIME	25 milliseconds
REWIND TIME	3 minutes (2,400 feet)

7.4.2. UNISERVO 16 Magnetic Tape Subsystem



The UNISERVO 16 Magnetic Tape Subsystem consists of a control unit and from one to sixteen magnetic tape units. Another control unit may be used to achieve simultaneous dual access operation when appropriate features are present on the magnetic tape units.

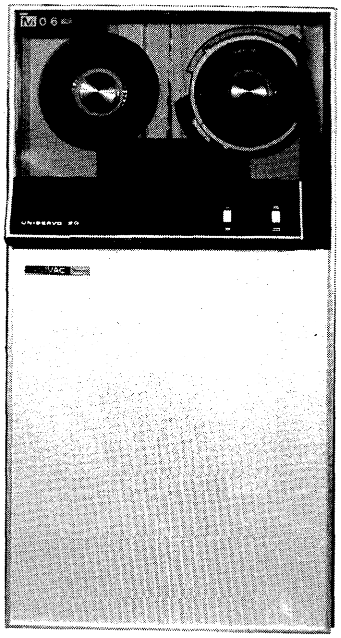
The UNISERVO 16 Magnetic Tape Unit also provides a power window as an additional operator convenience. The 120-inch-per-second tape speed provides for a transfer rate of 192,000 frames per second.

Data may be recorded in variable-length blocks under program control with character and block (horizontal and vertical) parity. A read-after-write head allows immediate verification of all data written. Under the control of the software input/output handler, repeated read and write operations are undertaken in an attempt to recover from an error.

CHARACTERISTICS

RECORDING DENSITY (PE)	1600 bpi
RECORDING DENSITY (NRZI)	200, 556, or 800 bpi
TRANSFER RATE (PE)	192,000 frames per second
TRANSFER RATE (NRZI)	24,000; 66,720; 96,000 frames per second
TAPE SPEED	120 inches per second
TAPE WIDTH	0.5 inch
TAPE LENGTH (MAX.)	2400 feet
BLOCK LENGTH	Variable
INTERBLOCK GAP	0.75 inch (7-track) 0.6 inch (9-track)
INTERBLOCK GAP TIME (7-TRACK)	6.25 milliseconds (nonstop) 9.25 milliseconds (start/stop)
INTERBLOCK GAP TIME (9-TRACK)	5.0 milliseconds (nonstop) 8.0 milliseconds (start/stop)
REVERSAL TIME	10 milliseconds
REWIND TIME	2 minutes (2400 feet)
DUAL DENSITY	Feature available

7.4.3. UNISERVO 20 Magnetic Tape Subsystems



The UNISERVO 20 Magnetic Tape Subsystem consists of a control unit and from one to sixteen magnetic tape units. Another control unit may be used to achieve simultaneous dual access operation when appropriate features are present on the magnetic tape units.

The UNISERVO 20 Magnetic Tape Units provides operational conveniences such as power window, automatic tape threading, and the ability to use a wrap-around tape cartridge. The 200-inch-per-second tape speed provides for a transfer rate of 320,000 frames per second. Rewind rate is 500 inches per second providing a rewind time of 60 seconds for a full 2400-foot reel of tape.

The UNISERVO 20 Control Unit contains all the necessary logic and storage facilities for data control transfer between the 1100/40 System I/O channel and the tape units; the word and command formats are compatible with those required by the 1100/40 System and the tape units.

CHARACTERISTICS

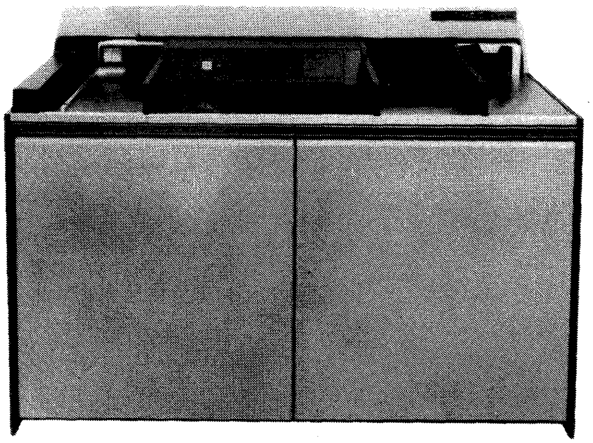
TRANSFER RATE (PE)	320,000 frames per second
RECORDING DENSITY (PE)	1600 bpi
TAPE SPEED	200 inches per second
TAPE WIDTH	0.5 inch
TAPE LENGTH (MAX.)	2400 feet
BLOCK LENGTH	Variable
INTERBLOCK GAP	0.6 inch
TRACKS ON TAPE	9 tracks, 8 data, 1 parity
UNITS PER CONTROL	16
STANDARD FEATURES	Backward read, automatic tape threading, power window, cartridge loading, quick release hub
INPUT/OUTPUT CHANNELS REQUIRED	1 or 2
REWIND TIME	1 minute (2400 feet)

7.5. BYTE INTERFACE PAPER PERIPHERALS

The following paper peripherals are connected to the 1100/40 System via the SPERRY UNIVAC Communications/ Symbiont Processor (C/SP), or the SPERRY UNIVAC Multi-Subsystem Adapter (MSA):

SPERRY UNIVAC 0716 Card Reader	– MSA, or C/SP
SPERRY UNIVAC 0770 Printer	– MSA, or C/SP
SPERRY UNIVAC 0604 Card Punch	– MSA, or C/SP
SPERRY UNIVAC 0920 Paper Tape Reader and Punch	– C/SP

7.5.1. SPERRY UNIVAC 0716 Card Reader Subsystem



The SPERRY UNIVAC 0716 Card Reader Subsystem includes a self-contained control unit and synchronizer that regulates flow of data and control signals to and from the reader mechanism. This control unit is attached to an MSA or to a C/SP by means of the multiplexer channel.

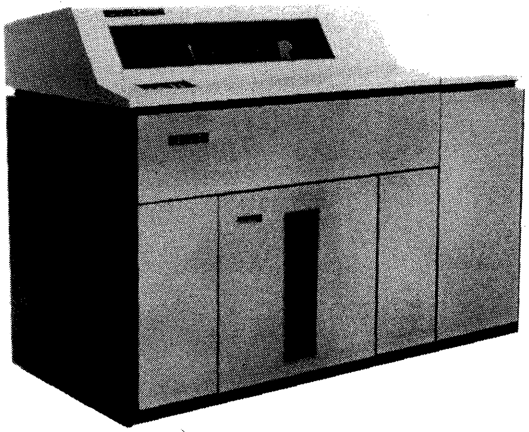
The 0716 Card Reader Subsystem operates at a rate of 1000 cards per minute on a column-by-column basis. The read-check feature is standard to ensure correct input. Information read from the card is transferred to the processor in either image mode or translate mode, which includes EBCDIC, ASCII, or compressed code. Image mode and selection of any one of the translate modes are standard features. The optional dual translate feature permits an additional selection from the two remaining choices offered by the translate mode. A validity check feature, checks for multiple punches in row one through seven.

Two output stackers provide the means for error selection as a standard feature in addition to the capability of stopping on error. An optional feature, alternate stacker fill, provides the capability of stacking 4000 cards: when stacker A is filled, the reader automatically begins to fill stacker B. The stop-on-error feature may be used with alternate stacker fill. The stacker carrousel wheel decelerates and stacks the cards at a rate which maximizes card handling care.

CHARACTERISTICS

CARD READING SPEED	1000 cards per minute
INPUT HOPPER CAPACITY	2400 cards
OUTPUT STACKER CAPACITY	2 stackers – 2000 cards each
READ MODES	Image Mode: 160 6-bit characters per card Translate mode: EBCDIC – 80 characters per card ASCII – 80 characters per card Compressed code – 80 characters per card Fieldata – 80 characters per card
OPTIONAL FEATURES	Validity check Alternate stacker fill Dual translate End of file Read buffer (when used on MSA)

7.5.2. SPERRY UNIVAC 0770 Printer Subsystem



The SPERRY UNIVAC 0770 Printer Subsystem is a freestanding, self-contained unit, that interfaces with the 1100/40 System via an MSA, or a C/SP.

The 0770 Printer Subsystem is a family of printers that feature an easily replaceable print band cartridge. The family is comprised of three printers that print at a rate of 800, 1400, or 2000 lines per minute using a standard 48-character set. Other character sets are available. The character set is located on a continuous metal band which travels in a horizontal direction across the front of the printed form. This printing method assures optimum print quality through close control of print registration. The metal band contains 384 characters which are usually grouped in repeating arrays. For example, a 48-character set is repeated on the band eight times.

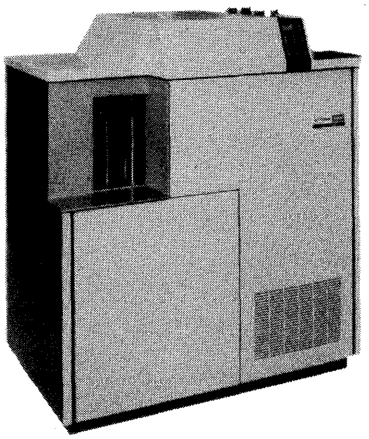
In addition to the standard 132 print position, the subsystem can be ordered with an optional 160-print-position feature. The 160 print positions offer more opportunities for increasing throughput with the use of "two-up" and "three-up" forms.

More than 20 standard print cartridges are available in up to four print fonts. The print cartridge case serves as the means for the operator to remove and replace the character set used on the printer in a manner similar to operations performed with magnetic disc pack covers.

CHARACTERISTICS

	0770–00 PRINTER SUBSYSTEM	0770–02 PRINTER SUBSYSTEM	0770–04 PRINTER SUBSYSTEM
PRINTING SPEED (SINGLE-LINE SPACING)	800 lpm – 48 character set 1435 lpm – 24 character set	1400 lpm – 48 character set 2320 lpm – 24 character set	2000 lpm – 48 character set 3000 lpm – 24 character set
MAXIMUM FORMS SLEW RATE	50 inches per second	75 inches per second	100 inches per second
CHARACTERS PER PRINT CARTRIDGE		384	
PRINT POSITIONS PER LINE		132 or 160	
SINGLE LINE SPACE TIME		8.75 milliseconds	
HORIZONTAL SPACING OF CHARACTERS		10 per inch	
VERTICAL LINE SPACING		6 or 8 lines per inch under program control	
FORM WIDTH		3.5 to 22 inches	
FORM LENGTH		To 24 inches	
FORM ADVANCE CONTROL		Vertical format buffer under program control	

7.5.3. SPERRY UNIVAC 0604 Card Punch Subsystem



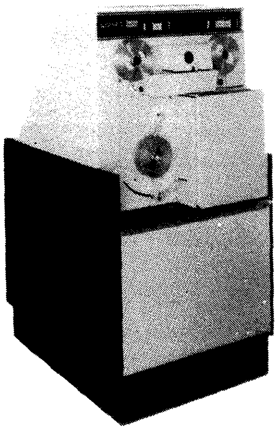
The card punch operates at a rate of 250 cards per minute on a row-by-row basis (12 punching positions per card). Standard features include processing 80-column cards in either punched card code or main storage image code modes. Output cards can be directed to either stacker under control of program.

The card punch includes a self-contained control unit and a synchronizer which regulates the flow of data and control signals to and from the punch mechanism. The control unit is connected via an MSA or a multiplexer channel of a C/SP.

An optional feature is the inclusion of the read/punch feature. The read/punch option allows prepunched cards to be sensed and read into the punch buffer from a prepunch station.

CHARACTERISTICS	
CARD PUNCHING SPEED	250 cards per minute
INPUT HOPPER CAPACITY	1000 cards
OUTPUT STACKER CAPACITY	3 stackers — 1000 cards per stacker
PUNCH MODES	Image mode — 160 6-bit characters per card Translate mode — 80 characters per card
OPTIONAL FEATURE	Read before punching (not software supported)

7.5.4. SPERRY UNIVAC 0920 Paper Tape Subsystem



The SPERRY UNIVAC 0920 Paper Tape Subsystem consists of a control unit, a paper tape reader with a reader synchronizer and/or a paper tape punch with a punch synchronizer. The control unit provides the necessary synchronization and interface between the reader and/or punch synchronizer and the C/SP multiplexer channel. The synchronizer unit regulate the transfer of data between the tape reader or tape punch and the control unit. The entire subsystem is housed in a freestanding cabinet and is connected by means of one of the eight physical connections provided in the standard multiplexer I/O channel.

The control unit handles paper tape codes of five, six, seven, or eight levels. During the reading or punching of less than eight levels, all data is enclosed in the least significant bit positions of the byte, and the control unit zerofills any unused most significant bit positions. The reading and punching of binary data from paper tape is possible and is selected by program option. When reading and punching binary data, the program connector is bypassed and all eight levels of the tape character are transferred to main storage with tape channels 1 through 8 corresponding to bit positions 7 through 0, respectively. The translation of all paper tape codes to internal code is performed by the software.

Simultaneity of read and punch operations is accomplished by connecting two control units to the paper tape subsystem.

Spooling features are optional for both the tape reader and tape punch. The tape spooler hubs for the tape reader can accommodate snap-on supply and take-up reels of 5-inch diameter (300-foot capacity). The tape take-up spooler hub for the tape punch can accommodate snap-on reels of 5-inch diameter; a larger hub is used to accommodate snap-on reels of 8-inch diameter (1000-foot capacity).

CHARACTERISTICS	
TAPE READING SPEED	300 characters per second (with tape punched 10 characters per inch)
TAPE PUNCHING SPEED	110 characters per second (with tape punched 10 characters per inch)
TAPE WIDTH	11/16 inch or 1 inch
PAPER TAPE CODES	5-level (11/16 inch tape) 5-, 6-, 7-, or 8-level (1 inch tape)
AVERAGE REWIND ON TAPE SPOOLER	40 inches per second

7.6. SPERRY UNIVAC MULTI-SUBSYSTEM ADAPTER

The MSA enables byte-oriented peripheral devices to operate with the word oriented **1100/40** System.

Mixtures of up to eight paper peripherals may be attached to the MSA.

Mixtures of disc subsystems, magnetic tape subsystems, and paper peripherals on a single MSA are not recommended due to throughput considerations.

The basic MSA can interface one 1100/40 System I/O channel with up to eight peripheral control units. The MSA can be expanded by use of the SPI feature to interface with up to four 1100/40 System I/O channels (useful in Multiprocessor System Configuration). A second independent MSA and all associated features can be added to the original MSA cabinet.

A function buffer expansion feature is required for operation with the SPERRY UNIVAC 8425 Disc Subsystems. This feature provides six function buffers which allows expanded command chaining capability.

Another feature required for the 8425 Disc Subsystem is the search identifier register. This feature provides storage for twelve bytes of search data.

Four translation features are available for the MSA. The Fieldata translator provides translation of Fieldata code to and from a 6-bit subset of ASCII. The EBCDIC-FD translator provides translation of Fieldata code to and from a 64-character subset of EBCDIC. Two translators may be installed in an MSA. Each translator may be connected to from one to four I/O channels, but is restricted to one type of translator per channel.

7.7. SPERRY UNIVAC COMMUNICATION/SYMBIONT PROCESSOR

When the C/SP is used as a symbiont processor, it controls the transfer of data between the peripheral subsystems and the **1100/40** System. In this application, the I/O subroutines (symbionts) are run in the C/SP thus removing this burden from the host system. This results in a saving of both time and storage in the **1100/40** System.

Concurrent with controlling the peripherals, the C/SP can control communications between the **1100/40** System and remote terminals.

8. COMMUNICATIONS EQUIPMENT

8.1. GENERAL

There is a wide variety of methods for communicating with the SPERRY UNIVAC **1100/40** Systems. Data transfer rates can vary widely, and many communications terminals can be multiplexed to one remote terminal which has direct high speed access to the processor. The following lists typify the wide range of equipment available for data communications with a **1100/40** System.

- Onsite Communications Equipment
  - SPERRY UNIVAC General Communications Subsystem
  - SPERRY UNIVAC Communications/Symbiont Processor
- Remote Communications Equipment
  - SPERRY UNIVAC Data Communications Terminal (DCT) 1000
  - SPERRY UNIVAC Data Communications Terminal (DCT) 500
  - UNISCOPE 100 Display Terminal
  - UNISCOPE 200 Display Terminal
  - SPERRY UNIVAC 9200/9300 System

8.2. ONSITE COMMUNICATIONS EQUIPMENT

8.2.1. SPERRY UNIVAC General Communications Subsystem

The SPERRY UNIVAC General Communications Subsystem (GCS) enables a **1100/40** System to receive and transmit data by way of any common carrier at any of the standard rates of transmission up to 50,000 bits per seconds. It can receive data from or transmit data to the various speed lines in any combination consistent with system throughput.

The GCS Subsystem, as illustrated in Figure 8–1, consists of three principal elements:

1. Communications Terminal Controller (CTC)

   The CTC is a multiplexing device that provides the means for the processor to communicate over transmission facilities with a number of terminals. By switching quickly from one line to another (within 4 microseconds), the CTC can be compared to a switchboard in selecting and multiplexing data exchange between the processor and communications devices.

2. Communications Terminal (CT)

   The CT performs the communications functions; such as serializing, staticizing, character recognition, synchronization, character parity check and generation, block parity check and generation, and dialing. The CTC can accommodate from 1 to 32 CTs. Each CT contains two (one input and one output) communications circuits. All CTs require a communications interface (CI) to provide interconnection to the data sets, automatic calling units, or telegraph lineș. The CT will arrange data in the format required by the processor or in the format demanded by the circuit with which the terminal is designed to operate.

3. Communications Interface (CI)

   The CI makes the necessary conversion between the electrical operating levels of the CTs and those of the communications line with which the CIs are designed to operate. The type of CIs required are dependent on the type of communications circuit or service to be used.

A GCS Subsystem may be connected to any input/output (I/O) channel for multiplexing up to 32 CT/CI pairs to that channel.

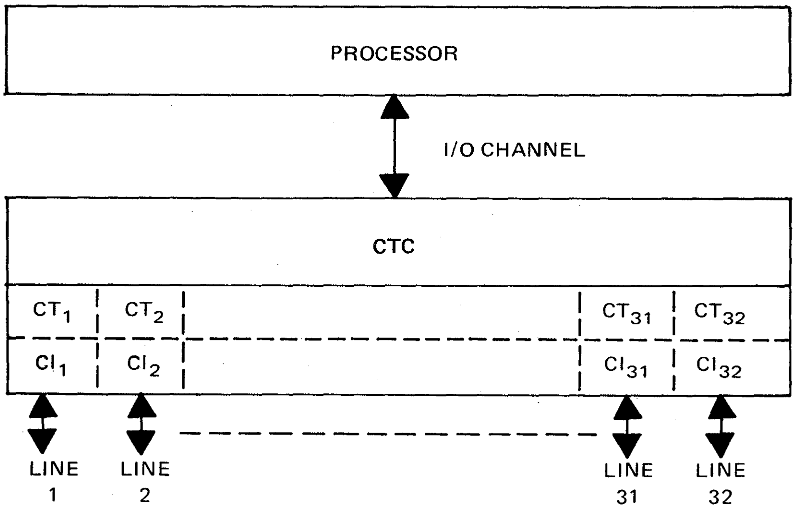


Figure 8–1. GCS Subsystem

There are three basic types of CTs:

1. Synchronous

2. Asynchronous

3. Dial

There are four basic types of CIs:

1. Telegraph (dc loop)

2. Modem

3. Dial

4. High Speed (wideband)

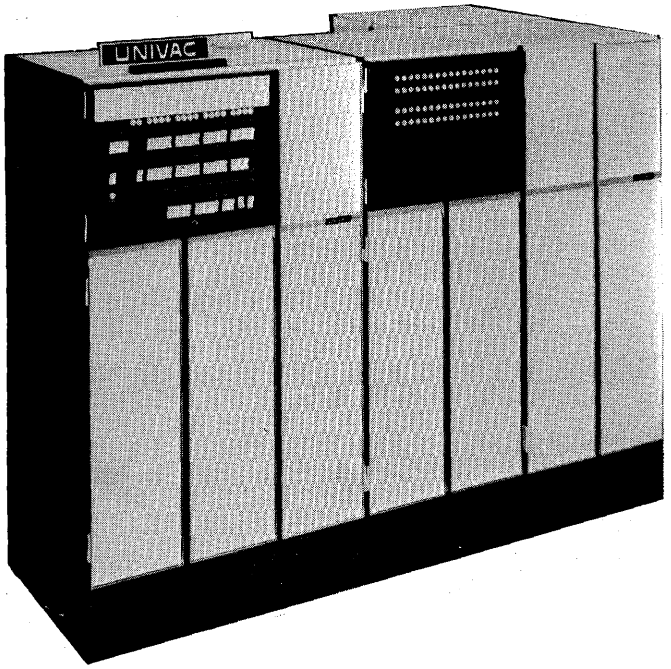
Each CT/CI combination is readily adaptable to the speed and character size of the type of line with which it is to operate. With the exception of the CT/CI Dial type, each CT/CI pair may operate in simplex, half duplex, or full duplex mode. The CT/CI enables the processor to establish communications with remote terminals through the common carrier's switching network.

Characteristics of the subsystem are summarized below.

TYPE	SPEED	MODE	LEVEL
Asynchronous	45.45 bps to 2400 bps	Asynchronous	5, 6, 7 or 8
Synchronous	Up to 50,000 bps	Synchronous	5, 6, 7 or 8
Dial	Variable	Bit Parallel	4

bps = bits per second

8.2.2. SPERRY UNIVAC Communications/Symbiont Processor



The SPERRY UNIVAC Communications/Symbiont Processor (C/SP) is a high performance, internally programmed system which is intended to absorb the function of communications control. Its high speed internal operation and multipurpose I/O channels provide high throughput rates and interface with communications facilities and terminals.

In assuming control of all communications operation, the C/SP relieves the host computer of storage allocated to terminal handler programs and of time associated with communications interrupt processing, data formatting, data editing, data translation, and other communications tasks.

System throughput is increased and user turnaround time is decreased by virtue of the improved system performance offered by isolated, dedicated processor elements.

The concept of front-end processing offers efficiency by simplifying the interface between the host system and its peripheral subsystems. All communications lines appear as a common intelligent subsystem to the host. The C/SP effectively buffers the host from the infinite variety of remote terminal and communications line transmission disciplines.

The C/SP hardware was designed to be modular and flexible. A multifunction subsystem includes special emphasis on high volume throughput. Special channels accommodate, with a high degree of efficiency, the varying needs of communication terminals. The configuration (see Figure 8–2) includes the following:

- Processor Unit
  - Processor
  - 16 general purpose registers

  - Maintenance panel
  - Interval timer
  - Special device channel
  - SPERRY UNIVAC 1100 Series adapter channel

- Storage Unit
  - 32K to 131K bytes storage
  - Storage protection feature

- Optional Features
  - Expansion to 131K bytes
  - One additional 1100 Series adapter channel
  - Multiplexer channel (for the paper peripherals, if used)
  - Selector channel (tape or disc subsystems, if used)
  - One or two general purpose communications channels (GPCC)
  - Dialing adapters (uses one CLT position)
  - Asynchronous timing assemblies

The SPERRY UNIVAC 1100 Series Operating System fully supports the following Sperry Univac peripherals connected to the C/SP multiplexer channel:

- SPERRY UNIVAC 0604 Card Punch Subsystem
- SPERRY UNIVAC 0716 Card Reader Subsystem
- SPERRY UNIVAC 0768 Printer Subsystem
- SPERRY UNIVAC 0770 Printer Subsystem
- SPERRY UNIVAC 0920 Paper Tape Subsystem

The SPERRY UNIVAC 1100 Series Operating System fully supports either of the following Sperry Univac peripherals connected to the C/SP selector channel:

- SPERRY UNIVAC 8425 Disc Subsystem
- UNISERVO 12/16 Magnetic Tape Subsystem

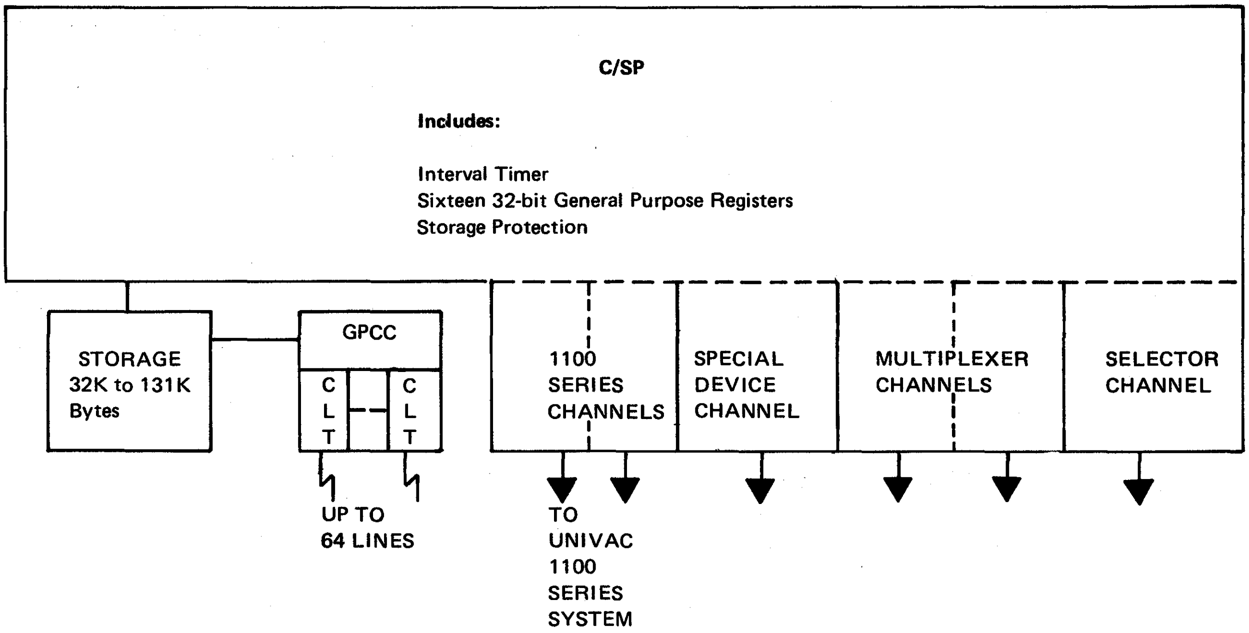


Figure 8–2. UNIVAC Communications/Symbiont Processor (C/SP) Configurator

8.2.2.1. Processor

The processor portion of the C/SP provides the flexibility that is required to control the I/O data flow and to perform message processing, as necessary, in an online peripheral or a communications environment. Major features of the processor include the following:

- 52 half-word and full-word instructions;
- sixteen 32-bit general purpose registers, external to storage;
- attached processor maintenance panel;
- I/O interrupt and data priority controls;
- variable interval timer;
- halfword basic data path;
- multilevel interrupt;
- 630-nanosecond cycle time;
- basic binary add (register to indexed storage) instruction time of 2.52 microseconds (four cycles);
- binary add instruction (register to register) time of 1.26 microseconds (two cycles);
- zero time indexed base and displacement calculation; and
- double indexing.

The control section of the processor regulates the sequence in which instructions are executed, interprets and controls the execution of each individual instruction, initiates cycling of main storage, performs required storage address modification and indexing, and determines the different processor modes of operation. All of the hardware aspects of interrupt handling, error checking, and protection are also performed by the control section.

The arithmetic section performs all data manipulations including logical and numerical arithmetic, data comparisons, and shifting. The arithmetic section also performs single or double indexing of operand addresses. Arithmetic operations are performed in the two complement form. A fixed-point arithmetic operand can be either a 32-bit fullword or a 16-bit halfword. The sign of a fixed-point operand is always the leftmost bit of the operand. When accessed from storage, a half-word fixed-point number is always expanded to a right-justified fullword; the sign is extended to the left.

Logical operations on fixed-length operands are performed in registers. Logical operations include comparing, bit setting, bit testing, and bit manipulation.

The C/SP utilizes a set of 52 basic instructions that vary in format and length. The format, in general, is dictated by the operation to be performed and the location of the operands. Operands may be located in storage, in general purpose registers, or in the instruction itself. The length of an instruction is dictated by the format and is either a halfword or a fullword. All processor instructions must be on half-word boundaries in storage. Operand addresses in storage are on byte, half-word or full-word boundaries, depending upon the instruction. For example, if an operand for a particular instruction is a fullword, the operand address in storage must be on a full-word boundary.

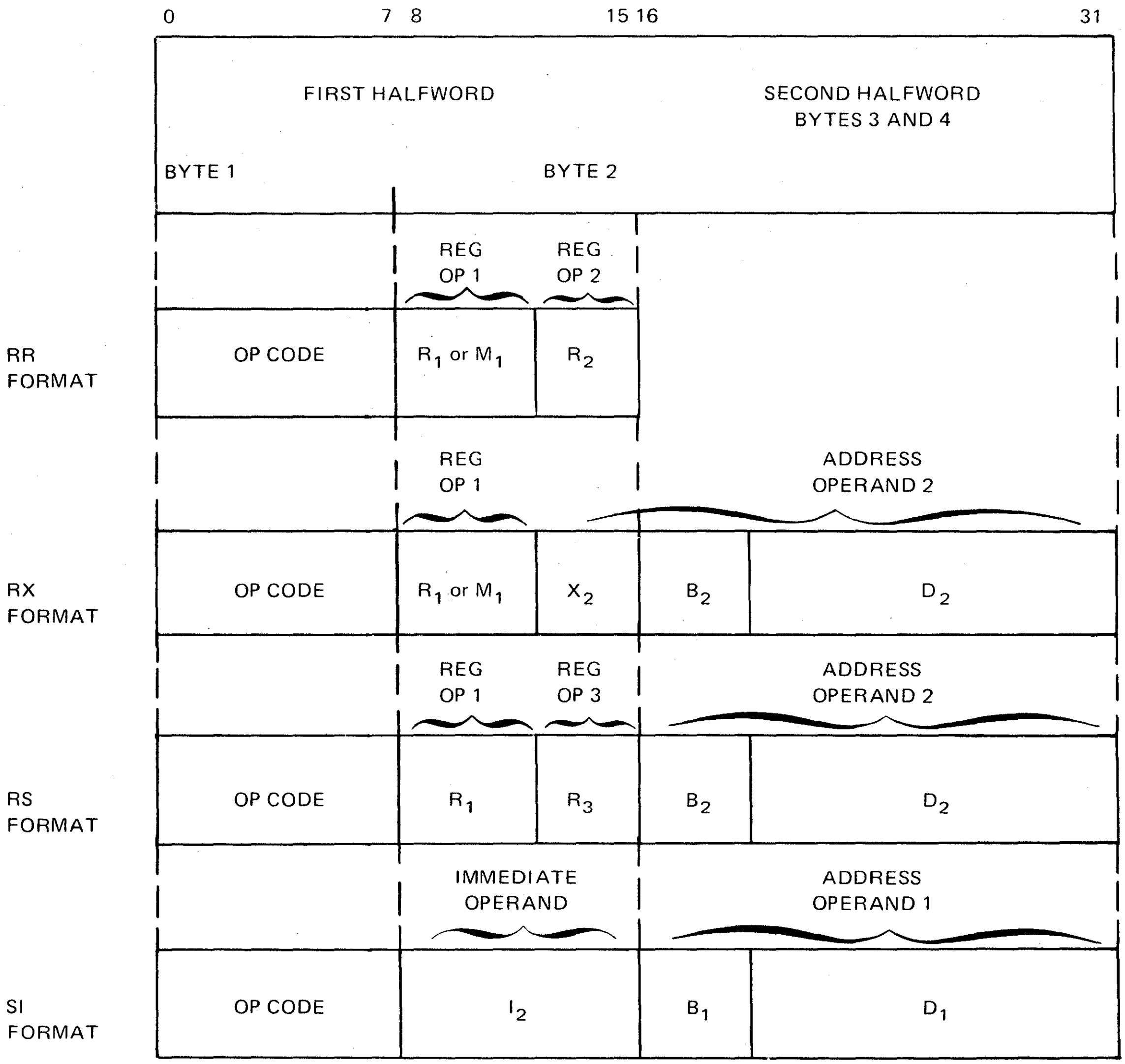
The four basic instruction formats that are used in the C/SP are illustrated in Figure 8–3 and are designated as follows:

- RR (Register to Register) Instructions
- RX (Register to Indexed Storage) Instructions
- RS (Register to Storage) Instructions
- SI (Storage and Immediate Operand) Instructions

Each format consists of an operation code (OP code) and two or more fields which specify, among other things, the addresses of operands (in storage or in the general purpose registers). Each field is identified by a letter followed by a subscript numeral. The numeral, in general, denotes the operand (1, 2, or 3) to which the field applies.

The C/SP instruction repertoire is listed in Table 8–1. The operation codes are expressed in hexadecimal (base 16); each code appears as two hexadecimal digits in the eight-bit OP code field of each instruction.

The interval timer, which utilizes a fixed-word location in storage, is a processor feature which provides interval timing and time of day information. Interval timer requests for service are made every 6 milliseconds. The interval timer provides an interrupt to the processor at a software specified interval in 6-milliseconds multiples. Interval timer requests may be serviced only at the end of a processor instruction execution prior to the processor staticizing the next instruction.



OP CODE	– Instruction operation code
R_1	– The number of the register addressed as operand 1, or a register which is the first register of a multiregister group
R_2	– The number of the register addressed as operand 2
R_3	– An expression representing a register which is the last register in a multiregister group
X_2	– The number of the register to be used as an index for operand 2 of an RX instruction
I_2	– The immediate data or device address used as operand 2 of a SI instruction
B_1	– The base register for operand 1
B_2	– The base register for operand 2
D_1	– The displacement for operand 1
D_2	– The displacement for operand 2
OP1	– Operand 1
OP2	– Operand 2
OP3	– Operand 3 (extended mnemonic repertoire)
M1	– Mask (extended mnemonic repertoire)

Figure 8–3. C/SP Instruction Formats

Table 8—1. Basic C/SP Instruction Repertoire (Part 1 of 2)

Functional Description	Mnemonic	OP Code (Hexadecimal)	Format*	Execution Time (Cycles)**
Add	A	5A	RX	4
Add Half-word	AH	4A	RX	4
Add	AR	1A	RR	2
Compare	C	59	RX	4
Compare Half-word	CH	49	RX	4
Compare	CR	19	RR	2
Divide Half-word	DH	53	RX	22
Load	L	58	RX	4
Load Half-word	LH	48	RX	4
Load	LR	18	RR	2
Multiply Half-word	MH	52	RX	20
Shift Left Single	SLA	8B	RS	3 + N1 (Note 2)
Shift Right Single	SRA	8A	RS	3 + N1 (Note 2)
Subtract	S	5B	RX	4
Subtract Half-word	SH	4B	RX	4
Subtract	SR	1B	RR	2
Store	ST	50	RX	5
Store Half-word	STH	40	RX	4
LOGICAL				
AND	N	54	RX	4
AND	NI	94	SI	5 (Note 1)
AND	NR	14	RR	2
Compare Logical	CL	55	RX	4
Compare Logical	CLI	95	SI	5 (Note 1)
Compare Logical	CLR	15	RR	2
Divide Polynomial	DP	81	RS	3 + N (Note 2)
Exclusive OR	X	57	RX	4
Exclusive OR	XI	97	SI	5 (Note 1)
Exclusive OR	XR	17	RR	2
Insert Character	IC	43	RX	3
Load Address	LA	41	RX	4
Move	MVI	92	SI	5 (Note 1)
OR	O	56	RX	4
OR	OI	96	SI	5 (Note 1)
OR	OR	16	RR	2
Shift Left Single Logical	SLL	89	RS	3 + N1 (Note 2)
Shift Right Single Logical	SRL	88	RS	3 + N1 (Note 2)
Store Character	STC	42	RX	4
Test Under Mask	TM	91	SI	5 (Note 1)

Table 8–1. Basic C/SP Instruction Repertoire (Part 2 of 2)

Functional Description	Mnemonic	OP Code (Hexadecimal)	Format*	Execution Time (Cycles)**
Branch and Link	BAL	45	RX	4
Branch and Link	BALR	05	RR	3
Branch on Condition	BC	47	RX	2
Branch on Condition	BCR	07	RR	1/2 NB/B
Branch on Count	BCT	46	RX	4
Branch on Count	BCTR	06	RR	2/3 NB/B
Branch on Index High	BXH	86	RS	6
Branch on Index Low or Equal	BXLE	87	RS	6
STATUS SWITCHING				
Halt and Proceed	HPR	99	SI	***3 (If No Halt)
Load PSW	LPSW	82	SI	***5 (Note 1)
Set Storage Key	SSK	08	RR	***3
Set System Mask	SSM	80	SI	***4 (Note 1)
Supervisor Call	SVC	0A	RR	8
INPUT/OUTPUT				
Start I/O	SIO	9C	SI	***6–24

*RR – Register to Register
RX – Register to Indexed Storage
RS – Register to Storage
SI – Storage and Immediate Operand
**1 storage cycle = 630 nanoseconds, all RX instructions add one cycle if double indexing
***Denotes Privileged Instruction

NOTES:

1. Number of cycles is one less if not indexing.

2. N = Number of shifts up to 16, N_1 = Number of shifts up to 31 (Module 16).

The interrupt system provides an automatic means of altering the C/SP processor to conditions arising from errors, end of I/O operations, specified time intervals, and unexpected conditions relating to abnormal system operation. The interrupt system directs the processor to the appropriate program which is responsible for interrogation and action upon the cause of the specific class of interrupt generated. The system permits the interruption of any task to process an interrupt of higher priority. Among the features of the interrupt system are:

- automatic tabling of communications channel interrupts;
- a dynamically alterable priority structure;
- automatic dispatch by interrupt class; and
- automatic program switching by interrupt class.

8.2.2.2. Storage

High performance storage is a basic part of the C/SP. Storage is located in one or two freestanding cabinets, depending upon the size of the storage capacity. Major features of main storage include the following:

- Capacity – 32,768 bytes minimum; 131,072 bytes maximum
- Cycle Time – 630-nanosecond read/write cycle
- Operating Mode – Nondestructive readout
- Storage Data Path – 18 bits wide (two eight-bit bytes and two parity bits)
- Parity – Odd parity (one parity bit per byte)
- Addressing – Zero time indexed base and displacement
– Double indexed
- Storage Protection – Program and I/O transfer

The addressing hardware accommodates a 17-bit address field which permits one-cycle addressing of 131,072 bytes. While the address field permits the addressing of each byte, the least significant bit of the address is not used to access the data from storage.

On a read cycle, the storage presents two bytes to the processor. If the particular reference requires byte addressing, the processor selects the appropriate byte based upon the least significant bit of the address field. The capability for partial write is provided; that is, one byte may be written without altering the other byte in the storage halfword.

The parity bit associated with each byte provides odd parity for that byte. Parity generation and checking are performed in storage. The parity bits are, however, presented to the C/SP processor or an appropriate channel on a read cycle.

Indexing is accomplished by creating the operand address through the addition of the contents of the registers specified in the X_2 and B_2 portions of the instruction (see Figure 8–3) to the value contained in the displacement portion (D_2). Double indexing, (that is, use of both X_2 and B_2) requires one additional storage cycle. When single indexing, the use of X_2, rather than B_2 (B_2=0), to obtain the operand consumes no additional time. Use of the general purpose registers for indexing involves an 18-bit add; the displacement in this add is right-justified. Access to 131K of storage is therefore achieved through indexing in this manner.

In addition to the fixed storage assignment, there may be several programs resident in C/SP main storage at any one time. It becomes necessary to restrict storage accesses by a program to the storage limits assigned to it.

Associated with main storage are a maximum of 64 three-bit registers called key storage registers. The storage is divided into a maximum of 64 blocks, each of which contain 2048 bytes. To each of these blocks is assigned a key storage register. The six most significant bits of a storage address are used to define the address of the key storage register associated with the block containing the storage address.

Storage is segmented by grouping together all blocks whose associated key storage registers have the same setting. Since there are three bit positions in a key storage register, a maximum of eight storage segments can be defined.

When a program is loaded, the program is assigned a unique program number. This number is then loaded into the key storage register that is associated with each 2048-byte block assigned to the program.

Storage protection against improper storage accessing is provided for during instruction execution and I/O transfers.

- Instruction Execution Protection

  When a program is scheduled for execution, the program number is loaded into a program status word (PSW) register that is uniquely identified with the program currently in operation. On each access to storage during processing, the program number in this register is compared with the contents of the key storage register that is associated with the storage address. If a match is made, the storage access is allowed; otherwise an error interrupt occurs.

- I/O Transfer Protection

  The number of the program requesting the I/O transfer is presented to the I/O channel. Upon transfer, the contents of the key storage register that is associated with the address to which the transfer is to be made is checked against the program number associated with the I/O channel. Again, a match of the key storage register and program number permits the transfer to take place; otherwise, an error interrupt occurs.

8.2.2.3. Channels

All information transmission in and out of the C/SP is handled by channels. A channel controls the operation of I/O devices and the transfer of data between devices and storage.

Among the outstanding features of the C/SP channels are:

- direct access to storage;

- independent operation;

- simultaneous operation;

- priority interchangeability.

The C/SP may contain up to seven channels, numbered 0 to 6. Priority of these channels increases in descending channel number order, with channel 0 having the highest priority. The C/SP is equipped with the following channel types.

- Special Device Channel (SDC)

  The primary function of the SDC is to provide the means for local program loading and maintenance of the C/SP by using the optional serial 80-column, 80 cards per minute, card reader device.

- 1100 Series Adapter Channel

  The 1100 Series Adapter Channel (intercomputer adapter channel) provides an interface for direct connection of the C/SP to an I/O channel of a 1100/40 Processor. The maximum transfer rate is in the excess of 300,000 words (36 bits each) per second.

- Multiplexer Channel

  The multiplexer channel provides the capability of attaching all currently available SPERRY UNIVAC 9000 Series peripheral devices, which operate on this channel, to the C/SP.

- Selector Channel

  The selector channel provides the capability of attaching the SPERRY UNIVAC 8425 Disc Subsystem or the UNISERVO 12/16 Magnetic Tape Subsystems, which operate on this channel, to the C/SP.

- General Purpose Communications Channel (GPCC)

  The GPCC performs such functions as multiplexing the various CLTs so that one CLT may be serviced at a time, recognizing special characters and sequences of characters, checking character parity, coordinating all data transfers to and from storage, and executing other necessary operations.

  The CLTs perform the function of assembly and disassembly of data characters for proper reception from and transmission to a communication line; detection of certain conditions of the communications line such as loss of carrier, a ringing indication, and others; and establishment of character synchronization.

  The CLTs handle a wide range of communications with rates up to 50 kilobytes per second. However, the CLTs must be selected so that the total combined rate of service requests (one per byte) is no more than 50,000 per second. When the GPCC is operated at this maximum rate, somewhat less than 40 percent of all available storage cycles are utilized for this purpose.

  The GPCC is the link between storage and the CLTs and provides the data path and control for CLTs as they communicate with storage. The single data path can be time shared by as many as 64 positions, which need not have identical CLTs. A full duplex CLT uses two multiplexer positions; a half duplex or simplex CLT utilizes only one multiplexer position.

  The GPCC is equipped to analyze each data character or sequence of characters which is transmitted through the GPCC and to act upon these characters in a manner that is a program-changeable function of the line to which the GPCC is connected. The GPCC also interfaces with the C/SP processor to service Start I/O (SIO) instructions and interrupts. Associated with the GPCC is a display panel which contains two active line indicators (output and input) for each CLT. The indicator is on when the corresponding CLT data line is in a spacing condition.

  The multiplexer portion of the GPCC accepts up to 64 simultaneously presented service requests from the CLTs plus an external function (XF) request from another portion of the GPCC. The multiplexer selects one request by connecting the selected CLT to the GPCC. When all necessary information has been interchanged, the multiplexer is cleared and can immediately accept another request. The multiplexer can accommodate a maximum of 32 full-duplex CLTs or 64 half-duplex CLTs. An area in storage called a buffer control word (BCW) is associated with each position on the multiplexer and is used to store status, control information, and data address information for the particular position.

When information is to be transferred during an I/O operation, the CLT requests service from the GPCC and, when priority permits, sends the CLT address to GPCC. The GPCC uses the address to select the associated BCW which is loaded into the channel and now controls the channel operation until the information is transferred. Then the BCW, in general changed by the channel operation (for example, address incrementation), is returned to main storage and the GPCC facilities are released. The BCWs remember the current state of the various positions.

The C/SP is intended to operate in an environment which can involve many different line discipline procedures. Many such procedures have been long established and must be handler unchanged by the C/SP. To avoid a multiplicity of tailored CLTs operating through the GPCC, the BCW is permitted to access a message discipline word (MDW). A chain of MDWs can be considered as a description of a given procedure, and the currently active MDW represents the position reached by a given line within that procedure. The chain of MDWs should not be modified once it has been loaded. Hence all lines with the same line discipline procedure may share a common chain of MDWs. An MDW contains, for example, parameters which control character parity checking, special character recognition (single or multiple), special character insertion, and other operations.

At various points throughout a procedure, it is necessary to present certain information to the controlling program. Since this information is dynamically changing, it must be stored at the desired point immediately. A normal interrupt is not sufficient since the processor is not always in a condition to accept an interrupt request. Four interrupt lists are provided in storage where communication interrupt words (CIWs) are stored. These lists are controlled by CIW list controls which are in fixed storage locations. A list is selected by a BCW or MDW and is usually assigned on a priority basis.

8.2.2.4. Programmed Systems Support

The software support provided for the C/SP is designed to provide complete flexibility for handling communications configurations with all types of terminal hardware while maintaining an expedient user interface. Coding efficiency is achieved by the utilization of a powerful instruction set at the assembly level. System macros are also provided to facilitate the user's requirements.

Software to integrate the C/SP effectively with the host processor system is included in the SPERRY UNIVAC 1100 Series Operating System and is controlled by system generation parameters.

The software package is divided into the following two segments:

- C/SP Operating System

  The C/SP operating system comprises various program modules which are specified by the user at system generation. When supplied elements are used, the following are included:

  - Terminal Management Supervisor (TMS)
  - Message Control Program (MCP)
  - Terminal Management Control Routine (TMCR)
  - Communication Control Routines (CCR)

  System interface is provided for inclusion of user versions of, or additions to, any element specified under the operating system.

- Support Programs – operating under the SPERRY UNIVAC 1100 Series Operating System

The following programs operate under control of the host processor executive system and are described in the paragraphs that follow.

- C/SP Assembler
- C/SP Element Collector
- C/SP Simulator
- C/SP Service Routines

The C/SP assembler is one-phase two-pass bootstrap assembler. The assembler is an efficient, easy-to-use, processor with macro capabilities. Each machine instruction and data form has simple, convenient representations in assembly language. The assembler translates this language into a form that can be executed by the processor. The rules that govern the use of the language are uncomplicated and can be easily applied by the programmer.

The C/SP element collector provides a means of collecting independent relative binary elements to produce an absolute program for execution in the C/SP. A relative binary element is an output of the assembler, as a result of translating C/SP assembler instructions. An absolute program is a program unit with no unresolved references which can be relocated in C/SP storage as an executable program.

The C/SP simulator is a SPERRY UNIVAC 1100 Series Assembler Language user program which runs under the operating system. The simulator accepts C/SP object code, simulates execution on the C/SP processor, and provides diagnostic printout to aid in debugging the C/SP program.

The following C/SP service routines are provided on the host processor.

- Initial Load of C/SP
- Program Load of C/SP
- Logging of Data for C/SP
- Console Communications
- Sign-on
- C/SP Storage Dump

8.3. REMOTE COMMUNICATIONS EQUIPMENT

8.3.1. UNISCOPE Display Terminals

Two SPERRY UNIVAC Display Terminal types are available with the 1100/40 Systems. These display terminals are:

UNISCOPE 200 Display Terminals
UNISCOPE 100 Display Terminals

The UNISCOPE Display Terminal is a alphanumeric display designed for a broad range of applications which require direct operator interaction with a centralized processor system. Due to its modular construction, the UNISCOPE Display Terminal can operate either as a data entry or as a display device. It can be conveniently located at the central processor site or at a remote station where it is connected to the system by way of telephone lines.

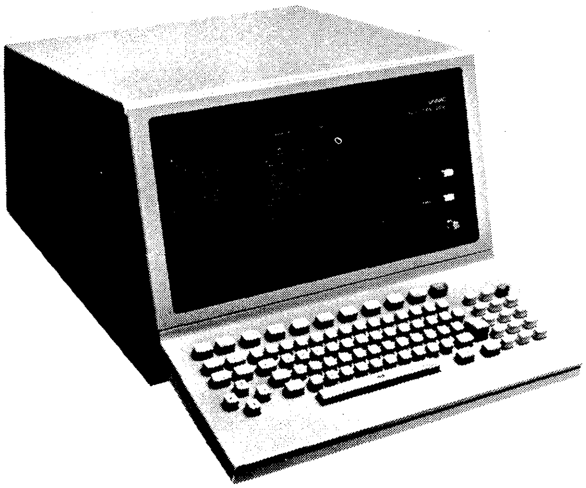
The UNISCOPE Display Terminal is a self-contained unit consisting of a cathode-ray-tube display screen, refresh storage, character generator, control logic, operator keyboard, and communications interfaces. A special interface for direct processor connection is available. Also available is an auxiliary interface that is used to connect up to eight devices to the UNISCOPE Display Terminal, such as the SPERRY UNIVAC Communications Output Printers or SPERRY UNIVAC Tape Cassettes. A variety of presentation formats are offered which provide a total display capacity of 480, 512, 1960, 1024, 1536, or 1920 USA Standard Code for Information Interchange (ASCII) characters. Each of these units is capable of displaying the complete ASCII set of 96 characters which include upper and lower case alphabetics. Hardware editing features enable the operator to completely edit any message prior to transmitting it to the processor.

Multiple UNISCOPE Display Terminals may be connected to a single communications line by means of a multiplexer. This general-purpose multiplexer is available with all the communications line interfaces available on the UNISCOPE Display Terminal, thus permitting a mixture of single units and multiple units on one communications system. The multiplexer also provides broadcasting of output messages to multiple devices.

The keyboard has been functionally designed to approximate the conventional electric typewriter, with its keyboard appearance, touch pressure, key travel, and slope characteristics. Typewriting speeds in excess of eighty words per minute can be accommodated by the keyboard. Because of its similarity to the standard typewriter, little additional training is required to operate it.

The keyboard includes cursor controls and editing keys, and the layout is right-left assignment balanced to efficiently distribute the work load. The keys are arranged for convenient function discrimination.

8.3.1.1. UNISCOPE 200 Display Terminal



The UNISCOPE 200 Display Terminal offers a variety of presentation formats which provide a total display capacity of 1536 or 1920 USA Standard Code for Information Interchange (ASCII) characters.

UNISCOPE 200 Display Terminals may be mixed in any combination with UNISCOPE 100 Display Terminals and SPERRY UNIVAC Data Communications Terminals (DCT) 1000 on a single line.

8.3.1.2. UNISCOPE 100 Display Terminal

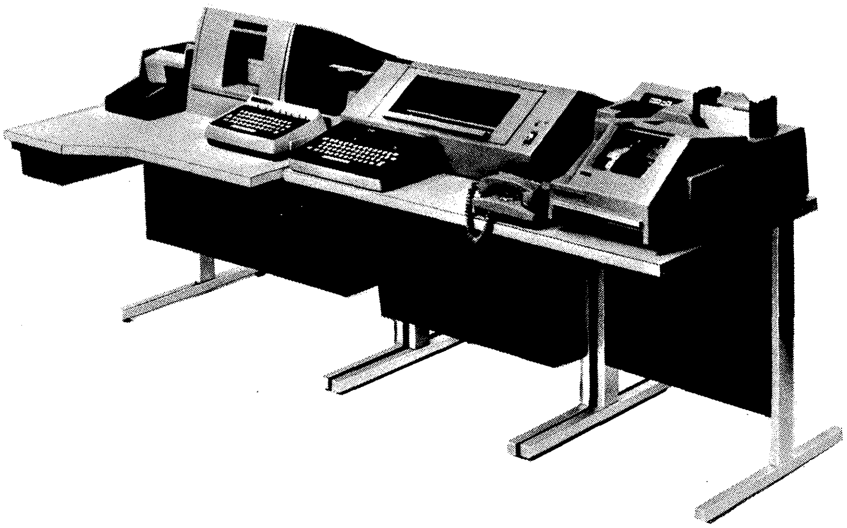
The UNISCOPE 100 Display Terminal offers a variety of presentation formats which provide a total display capacity of 480, 512, 960, or 1024 USA Standard Code for Information Interchange (ASCII) characters.

UNISCOPE 100 Display Terminals may be mixed in any combination with UNISCOPE 200 Display Terminals and SPERRY UNIVAC Data Communications Terminals (DCT) 1000 on a single line.

CHARACTERISTICS

	UNISCOPE 200 **Display Terminal**	**UNISCOPE 100** **Display Terminal**
DISPLAY	1536 or 1920 characters (64 per line, 24 lines; 80 per line, 24 lines) on 12-inch wide and 8-inch high screen. Characters are ASCII, and also include both upper and lower case alphabetics.	480, 512, 960 or 1024 characters (80 per line, 6 lines; 32 per line, 16 lines; 80 per line, 12 lines; 64 per line, 16 lines) on 10-inch wide and 5-inch high screen. Characters are ASCII, and also include both upper and lower case alphabetics.
KEYBOARD	Alphanumeric and symbolic with 8 cursor control keys and 5 editing keys	
STORAGE	7.2 microseconds cycle time, 7-bit ASCII code plus parity bit	
DATA TRANSMISSION	Up to 9,600 bits per second Half or full duplex Party line polling Nonsignificant space suppression Block transmission Message segmentation	
POWER	Standard office receptacles	

8.3.2. SPERRY UNIVAC Data Communications Terminal (DCT) 1000



The SPERRY UNIVAC Data Communications Terminal (DCT) 1000 is a fully buffered 30 character per second incremental printer which can be expanded to include a keyboard, card reader, card punch, paper tape reader/punch, and an auxiliary printer. The DCT 1000 transmits data or receives data from a local or remote processor or to a remote DCT 1000 in conversational or batch mode.

Two 160-character buffers are standard on the DCT 1000. These buffers facilitate the following:

- Automatic Blocking

  This eliminates complicated and time comsuming operator functions and minimizes training.

- Automatic Error Correction

  This eliminates manual correction protection procedures such as reloading cards and retyping input data.

- Error Free Output

  All messages are completely checked for character errors, block errors, duplicate blocks, or lost blocks. The result is that no errors are entered into the output medium.

- High Transmission Speeds

  The full capability of the line can be utilized since the transmission rate can be much higher than the I/O rate. On party line systems, this yields data throughput on a line which is the sum of the throughputs of the individual terminals.

The DCT 1000 has complete polling and address recognition capabilities allowing the processor to completely control multiple DCT 1000s on a single line. The terminals may be connected in a series string in different geographical locations or at a single point on the SPERRY UNIVAC Terminal Multiplexer.

The DCT 1000 can be tailored to complement the transmission facility which fits the application best. The following options are available:

Line Type	– Switched or private
Private Line	– Two-wire or four-wire
Mode	– Synchronous or asynchronous
Transmission Speed	– Asynchronous 300, 1200, or 1800 baud – Synchronous up to 4800 baud
Interface	– EIA RS-232 (synchronous or asynchronous) – MIL STD 188B (synchronous)
Direct Connection	– To CT or Data Communications Set without modems
I/O Channel	– Direct to processor I/O channel via terminal multiplexer.

The DCT 1000 transmission control procedures are completely compatible with those for the UNISCOPE 200 and UNISCOPE 100 Display Terminals. Therefore, these terminals can be intermixed on the same transmission line or on the same multiplexer. This mix and match capability yields an almost limitless number of configurations. Control can be achieved at the central processor with a single common handler.

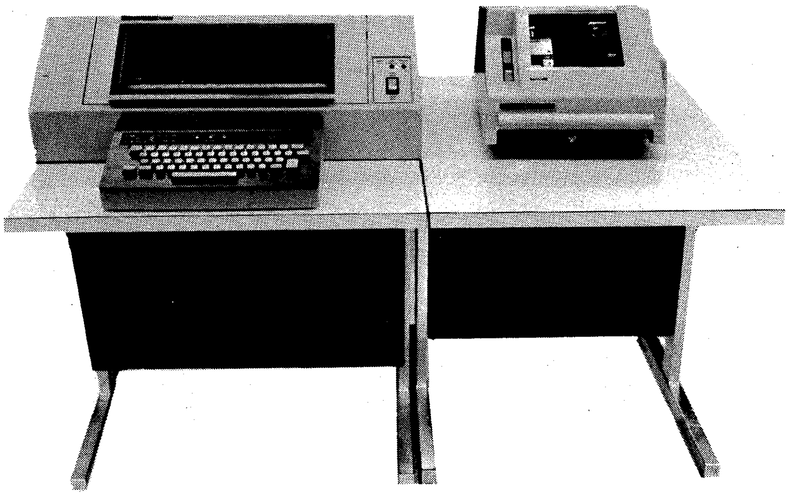
DCT 1000 (printer only) stations can be used to furnish hard copy for the UNISCOPE 200 and UNISCOPE 100 Display Terminals. The printing operation is not dependent on the display hardware and does not delay any operator functions at the display stations.

When the DCT 1000 is not transmitting or receiving data, it need not be idle. The DCT 1000 can be used offline to generate paper tapes, list cards, or for media conversion. Additionally, while the DCT 1000 is receiving or transmitting data online, the punch can be used offline.

CHARACTERISTICS

CARD READING SPEED	40 cards per minute
CARD PUNCHING SPEED	35 cards per minute
PRINTING SPEED	30 characters per second
PRINTING POSITIONS PER LINE	132 (adjustable tractor)
PRINTABLE CHARACTERS	63 plus space
PAPER TAPE SPEEDS	50 characters per second
BUFFER STORAGE	320 character capacity in two buffers, 160 characters each
TRANSLATOR SELECTIONS	ASCII H (Scientific) code A (Business) code Binary with additional feature
TRANSMISSION METHOD	Block by block
TRANSMISSION MODE	Half duplex; 2- or 4-wire (nonsimultaneous; two-way transmission)
TRANSMISSION FACILITIES	Voice-grade telephone toll exchange, or private line
TRANSMISSION RATE	Asynchronous 300, 1200, or 1800 bits per second; Synchronous 4800 bits per second
POWER	Standard office receptacle

8.3.3. SPERRY UNIVAC Data Communications Terminal (DCT) 500



The SPERRY UNIVAC Data Communications Terminal (DCT) 500 is an unbuffered, asynchronous keyboard/printer terminal similar in operation to a teletypewriter. The DCT 500 is, however, two to three times faster than a teletypewriter and it provides up to 132 print positions and five carbons. The DCT 500 can replace existing teletypewriters with little or no changes in the software handlers for point-to-point communications networks over voice-grade telephone toll lines or private lines. In a multiparty, polled environment, the DCT 500 operates in accordance with ASCII procedures.

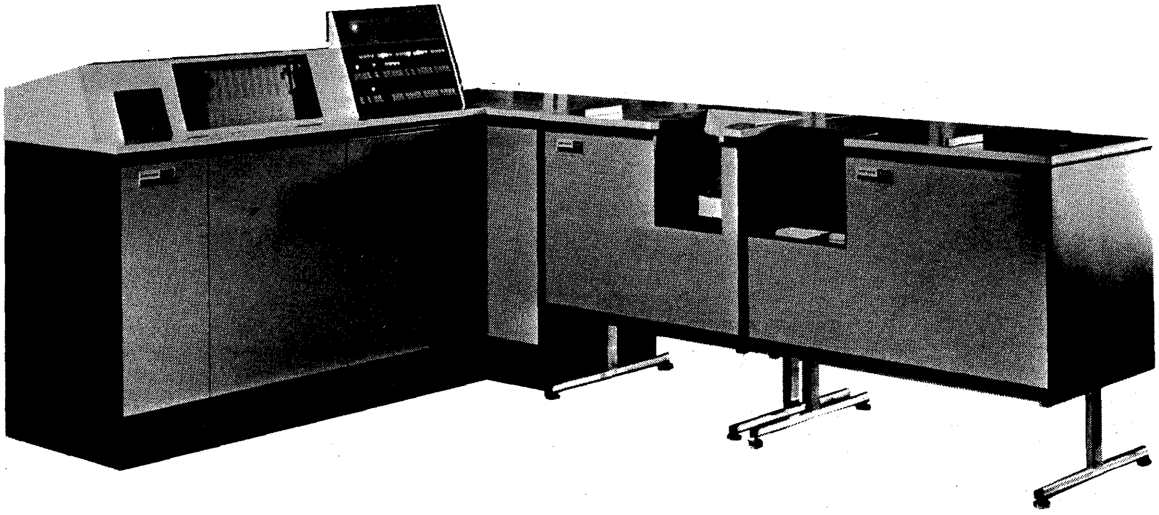
The DCT 500 can operate in a receive-only mode, a keyboard send/receive mode, or an automatic send/receive mode. The basic printer system (minimum equipment) can be expanded to include a keyboard and a 1-inch paper tape read/punch unit at any time. Additional optional equipment is available to allow for multi-station operation and the following optional features.

- Automatic Answering
- Automatic Operation
- Remote Control
- Master/Slave Operation
- Print Monitor
- Internal Modem
- Paper Tape

CHARACTERISTICS

TRANSMISSION CODE	8-level ASCII
INTERFACES	EIA Standard RS-232/CCITT Internal Modem
TRANSMISSION MODE	Half duplex or full duplex (2- or 4-wire)
TRANSMISSION RATE	110, 150, or 300 bits per second (selectable)
PRINTING RATE	30 characters per second
FONT SELECTIONS	ASCII, EBCDIC A (Business)/G (Scientific)
PRINTABLE CHARACTERS	63 plus space
PRINT POSITIONS PER LINE	132 (adjustable tractor)
PAPER TAPE READER/PUNCH RATE	50 characters per second
POWER	Standard office receptacle

8.3.4. Remote SPERRY UNIVAC 9200/9300 Subsystem



The minimum SPERRY UNIVAC 9200/9300 System consists of a central processor unit, 8K of main storage, and a printer. All other peripherals are options and must be specially ordered.

The remote 9200/9300 System requires a SPERRY UNIVAC Data Communications Subsystem (DCS) to enable it to communicate with the 1100/40 System.

The DCS subsystem provides communications capability for the 9000 Series Processors. Connected to a multiplexer channel, the DCS enables synchronous data transmission at speeds up to 50,000 bits per second between the 9200/9300 System and the 1100/40 System over standard communications circuits. The unit is physically small so that two of them can be mounted in space available in the 9200/9300 Processor's main frame.

The DCS is modular, permitting field modifications as demands for various options arise. As communications needs grow, different interfaces can be substituted to upgrade capabilities.

Its many features include the following:

- Automatic Error Checking

  The DCS checks character and message parity by sending either odd or even parity bits. Longitudinal redundancy can be checked by hardware or by user software.

- Self Testing

  The DCS may be tested under program control by connecting the output line to the input line to verify transmission and reception of data.

- Unattended Answering

  The subsystem responds to incoming calls from dialed lines without operator intervention.

- Variable Message Length

  A message may be of any length, from one character up to available storage size.

CHARACTERISTICS

	9200	9200 II	9300	9300 II
SYSTEM ORIENTATION*	Card/Disc	Card/Tape/Disc	Card/Tape/Disc	Card/Tape/Disc
BASIC MAIN STORAGE	8192 bytes	8192 bytes	8192 bytes	16,384 bytes
MAXIMUM MAIN STORAGE	16,384 bytes	32,768 bytes	32,768 bytes	32,768 bytes
MAIN STORAGE CYCLE TIME	1200 nanoseconds per byte	1200 nanoseconds per byte	600 nanoseconds per byte	600 nanoseconds per byte
ADD (DECIMAL) INSTRUCTION TIME (TWO 5-DIGIT NUMBERS)	104 microseconds	104 microseconds	52 microseconds	52 microseconds
MULTIPLY, DIVIDE, AND EDIT CAPABILITY	Optional	Optional	Standard	Standard
PRINT SPEED (INTEGRAL PRINTER)	250, 300, 500, or 600 lines per minute	250, 300, 500, or 600 lines per minute	600 or 1200 lines per minute	600 or 1200 lines per minute
MULTIPLEXER CHANNEL TRANSFER RATE	85,000 bytes per second	85,000 bytes per second	85,000 bytes per second	85,000 bytes per second
DATA COMMUNICATION SUBSYSTEM	Up to 8 duplex lines	Up to 8 duplex lines	Up to 8 duplex lines	Up to 8 duplex lines
REGISTERS	8 for processor functions 8 for I/O functions	8 for processor functions 8 for I/O functions	8 for processor functions 8 for I/O functions	8 for processor functions 8 for I/O functions

*Only card systems (not disc or tape) are supported by the SPERRY UNIVAC 1100 Series Executive System.

Characteristics for the DCS follow.

CHARACTERISTICS

SPEED AND FACILITIES	Low speed line – up to 300 bits per second Dial voice lines – 2000 bits per second Private voice lines – 2400 bits per second Broad-band lines – 50,000 bits per second
DATA CODING	Five to eight levels, plus parity
CHECKING	Odd or even message and character parity Longitudinal redundancy check is optional
MULTIPLEXER CHANNELS REQUIRED	One per subsystem

The SPERRY UNIVAC 1100 Series Executive System fully supports the following Sperry Univac peripherals connected to the SPERRY UNIVAC 9200/9300 multiplexer channel:

- SPERRY UNIVAC 0716 Card Reader Subsystem
- SPERRY UNIVAC 0768 Printer Subsystem
- SPERRY UNIVAC 0770 Printer Subsystem
- SPERRY UNIVAC 0920 Paper Tape Subsystem

Also software supported are the following card subsystems which are connected directly to the 9200/9300 System:

- SPERRY UNIVAC 0603 Card Punch Subsystem
- SPERRY UNIVAC 0711 Card Reader Subsystem

APPENDIX A. NOTATIONAL CONVENTIONS

a	Arithmetic register designator. In certain instructions, "a" may designate an I/O channel, the CAU to interrupt, a function code extension, and so on.
ACW	Access control word
BD	D-bank base of a PSR
BDX	6-bit extension of BD
BI	I-bank base of PSR
BIX	6-bit extension of BI
BS	Base selector of PSR
BDI	Bank descriptor index
BDP	Bank descriptor pointer
BDT	Bank descriptor table
BDW	Bank descriptor word
CAU	Command/arithmetic unit
CBR	Chain base register
CSR	Channel select register
E	A byte string whose starting word address is formed by summing the instruction u-field, the instruction specified index register and J register zero. $(u + X + J0_{ow})$. Field 0_b in J0 points to the byte within word.
F	A byte string whose starting word address is $(u + (X+1) + J1_{ow})$; Field 0_bin J1 points to the byte within the word.
f	Function code, bits 35–30 of instruction word.

G	A byte string whose starting word address is (u + (X+2) + $J2_{ow}$); field 0_b in J2 points to the byte within word.
GRS	General register stack
h	h designator; bit 17 of the instruction word. A value of 1 normally specifies incrementation of an index register.
IOAU	Input/output access unit
i	i designator, bit 16 of the instruction word. A value of 1 normally specifies indirect addressing.
J	J register, GRS addresses 106_8–111_8 or 126_8–131_8
j	Partial word designator or function code extension, bit positions 29–26 of the instruction word.
M	The byte count contained in field BB2 in staging register 3
MDW	Message discipline word
N	The byte count contained in field BB1 in staging register 3, GRS addresses 105_8 or 125_8
NI	Next instruction
P	The program address contained in the P register
PSR	Main processor state register
PSRE	Main processor state register extension
PSRU	Utility processor state register
PSRUE	Utility processor state register extension
R	R register, GRS addresses 100_8–137_8
Ra	R register specified by the a-field of an instruction.
SLR	Storage limits register
SLRM	Main storage limits register
SLRU	Utility storage limits register
SR1	Staging register 1 (R3), GRS addresses 103_8 or 123_8
SR2	Staging register 2 (R4), GRS addresses 104_8 or 124_8
SR3	Staging register 3 (R5), GRS addresses 105_8 or 125_8

U	The effective address or value of the operand after application of indexing and indirect addressing.
u	The base address of the operand (or the base of the actual operand) as coded in the u-field of an instruction.
X	Index register. A control register in the GRS specified by the x-field of an instruction.
X_a	Index register specified by the a-field of an instruction
X_i	Increment portion of an index register (bits 35–18)
X_m	Modifier portion of an index register (bits 17–0)
x	Index register designator
( )	Contents of
( )′	Complement of contents of
$\|(\ )\|$	Absolute value or magnitude
$(\ )_{17-00}$	Subscripts indicate the bit positions involved. A full word is normally not subscripted. Subscripts are also used to designate octal or decimal notation.
AND	Symbol denoting logical product, or logical AND
OR	Symbol denoting logical sum, or inclusive OR
XOR	Symbol denoting logical difference, or exclusive OR
→	Direction of data flow

APPENDIX B. SUMMARY OF WORD FORMATS

INSTRUCTION WORD

f	j	a	x	h	i	u
35 30	29 26	25 22	21 18	17	16	15 0

INDEX REGISTER WORD

X_i	X_m
35 18	17 0

MAIN PROCESSOR STATE REGISTER (PSR) WORD

INDEX REGISTER DESIGNATOR

D8 - - - - - - - D0	B1	D 10	D 9	BS	BD
35 27	26 18	17	16	15 9	8 0

QUARTER-WORD DESIGNATOR

MAIN PROCESSOR STATE REGISTER EXTENSION (PSRE) WORD

UNASSIGNED	D23 - - - - - - - - - - - - - - D11	BIX	BDX
35 25	24 12	11 6	5 0

UTILITY PROCESSOR STATE REGISTER (PSRU) WORD

UNASSIGNED

UNASSIGNED	BI			BS	BD
35 27	26 18	17	16	15 9	8 0

UTILITY PROCESSOR STATE REGISTER EXTENSION (PSRUE) WORD

UNASSIGNED	BIX	BDX
35 12	11 6	5 0

STORAGE LIMITS REGISTER (SLR) WORD*

I-PORTION UPPER LIMIT	I-PORTION LOWER LIMIT	D-PORTION UPPER LIMIT	D-PORTION LOWER LIMIT
35 27	26 18	17 9	8 0

BANK DESCRIPTOR WORD (BDW)

R	W		BIX/BI or BDX/BD	UPPER BOUNDARY I or D BANK	LOWER BOUNDARY I or D BANK
35	34	33	32 18	17 9	8 0

UNUSED

PROGRAM AREA DESCRIPTORS

BANK DESCRIPTOR POINTER (BDP) WORD

TABLE LENGTH	ABSOLUTE BANK DESCRIPTOR TABLE ADDRESS POINTER
35 24	23 0

SINGLE-PRECISION FIXED-POINT WORD

S	
35	34 0

DOUBLE-PRECISION FIXED-POINT WORD

S	
35	34 0

A

35 0

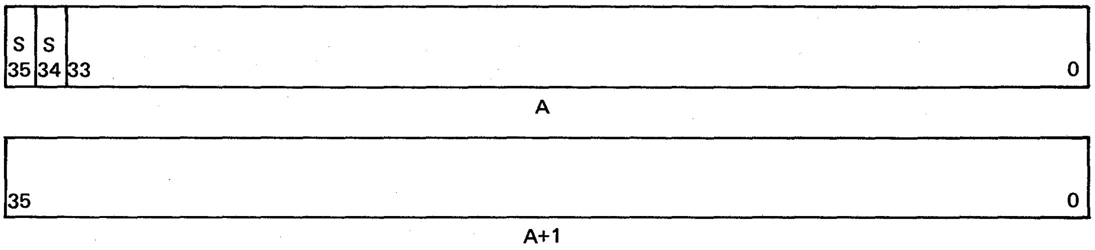
A+1

FIXED-POINT MULTIPLY SINGLE INTEGER RESULT

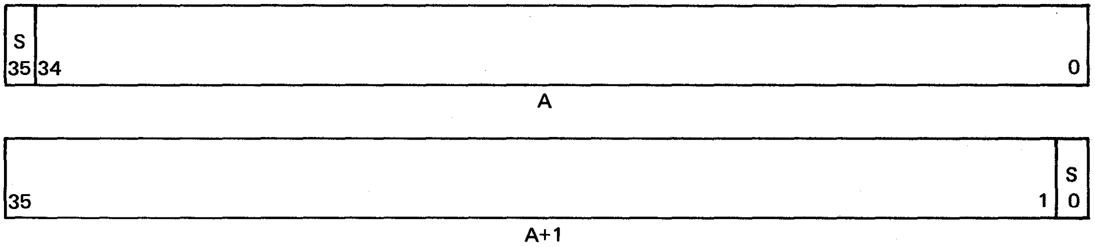
S	
35	34 0

**Format of utility storage limits register (SLRU) word is identical to the main storage limits register (SLR) word format.*

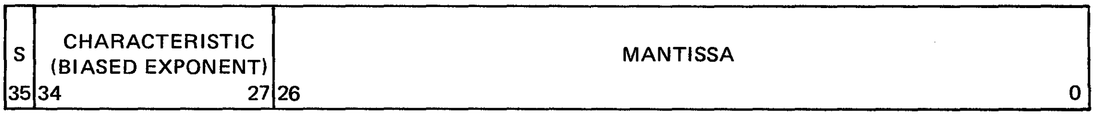
FIXED-POINT INTEGER MULTIPLY RESULT



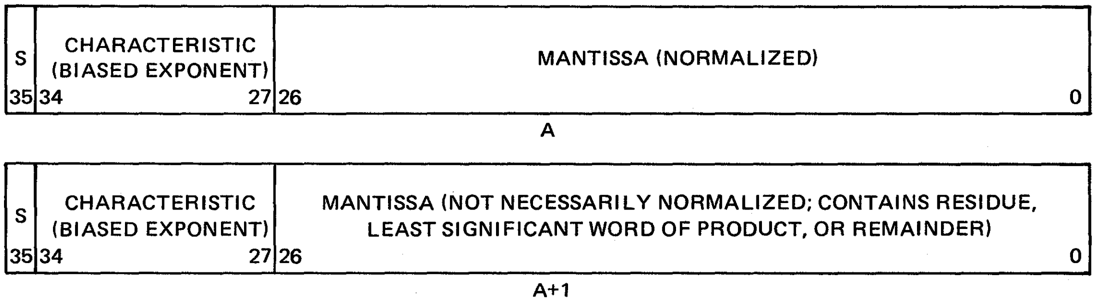
FIXED-POINT FRACTIONAL MULTIPLY RESULT



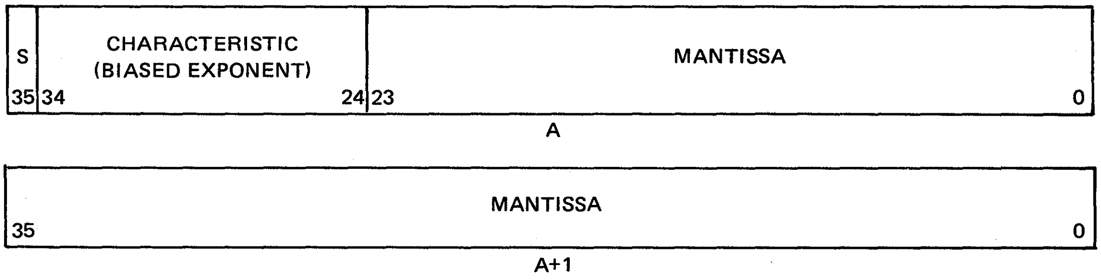
SINGLE-PRECISION FLOATING-POINT OPERAND



SINGLE-PRECISION FLOATING-POINT RESULT


S
CHARACTERISTIC (BIASED EXPONENT)
MANTISSA (NORMALIZED)
35
34
27
26
0
A
S
CHARACTERISTIC (BIASED EXPONENT)
MANTISSA (NOT NECESSARILY NORMALIZED; CONTAINS RESIDUE, LEAST SIGNIFICANT WORD OF PRODUCT, OR REMAINDER)
35
34
27
26
0
A+1

DOUBLE-PRECISION FLOATING-POINT OPERAND OR RESULT



ADD HALVES WORD FORMAT

S		S	
35	34 18	17	16 0
CARRY		CARRY	

ADD THIRDS WORD FORMAT

S		S		S	
35	34 24	23	22 12	11	10 0
CARRY		CARRY		CARRY	

ISI ACCESS CONTROL WORD

G	W	V
35 34	33 18	17 0

ESI ACCESS CONTROL WORD (half-word)

G	H	W	V
35 34	33	32 18	17 0

ESI ACCESS CONTROL WORD (quarter-word)

G	H	C	W	V
35 34	33 32	31 30	29 18	17 0

BYTE MANIPULATION STAGING REGISTER 1

BT 35 27									BS2	BS3	BS4
0	1	2	3	4	5	6	7	8	26 18	17 9	8 0

BYTE MANIPULATION STAGING REGISTER 2

BH0	BH1
35 18	17 0

BYTE MANIPULATION STAGING REGISTER 3

BB0	BB1	BB2	BB3
35 27	26 18	17 9	8 0

J REGISTER

I	M	W	E	I_w	I_b	O_w	O_b
35	34	33	32	31 21	20 18	17 3	2 0

APPENDIX C. INSTRUCTION REPERTOIRE AND INSTRUCTION TIMES

The estimated instruction times given below are a subset of the actual execution times. Actual execution times are a function of GRS conflicts, storage spigot conflicts, and internal CAU sequencing conflicts. Also, system parameters which effect actual execution times are conflicts for storage contention, storage characteristics (i.e., cycle time, access time, and service time), and cable lengths.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
00	–	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	3800	3800	NA
01	0–17	S, SA	Store A	(A) → U	300	440	NA
02	0–17	SN, SNA	Store Negative A	–(A) → U	300	440	NA
03	0–17	SM, SMA	Store Magnitude A	$\lvert(A)\rvert \rightarrow U$	300	440	NA
04	0–17	S, SR	Store R	$(R_a) \rightarrow U$	300	440	NA
05	0–17	SZ	Store Zero	ZEROS → U	300	440	NA
06	0–17	S, SX	Store X	$(X_a) \rightarrow U$	300	440	NA
07	00	SIA	Store Input Access Control Word	(A) → IACR; channel number per U_{5-0}	600	600	NA
07	01	SOA	Store Output Access Control Word	(A) → OACR; channel number per U_{5-0}	600	600	NA
07	02	SIP	Store Input Pointer Word	(A) → ICPR; channel number per U_{5-0}	600	600	NA
07	03	SOP	Store Output Pointer Word	(A) → OCPR; channel number per U_{5-0}	600	600	NA
07	04	LIA	Load Input Access Control Word	(IACR) → A; channel number per U_{5-0}	1800	1800	NA
07	05	LOA	Load Output Access Control Word	(OACR) → A; channel number per U_{5-0}	1800	1800	NA
07	06	LIP	Load Input Pointer Word	(ICPR) → A; channel number per U_{5-0}	1800	1800	NA
07	07	LOP	Load Output Pointer Word	(OCPR) → A; channel number per U_{5-0}	1800	1800	NA
07	10	LCB	Load Chain Base Register	If a=0, $(U)_{14-0} \rightarrow$ CBR; IOAU number 0 (for channel 0–23) If a=1, $(U)_{14-0} \rightarrow$ CBR; IOAU number 1 (channel 24–47)	600	600	NA

**See Appendix A for notational conventions.*

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
07	11	LPI	Load Processor Interrupt Pointer	if a=0, $(U)_{1-0} \rightarrow$ processor interrupt pointer register of IOAU number 0 (for channels 0–23); if a=1 $(U)_{1-0} \rightarrow$ processor interrupt pointer register of IOAU number 1 (for channels 24–47)	600	600	NA
07	12	LDJ	Load D Bank Base and Jump	Transfer the portions of the BDW specified by the BDP plus the BDI specified by (Xa) to PSR, SLR; P+1 → Xa modifier; jump to address U (on new PSR, SLR); P+1 → Xa modifier	2330	2330	NA
07	13	LIJ	Load I Bank Base and Jump	Transfer the portions of the BDW specified by the BDP plus the BDI specified by (Xa) to PSR, SLR; P+1 → Xa modifier; jump to address U (on new PSR, SLR); P+1 → Xa modifier	2330	2330	NA
07	14	LPD	Load PSR Designators	$U_{6, 5, 3-0} \rightarrow$ PSR; Bit 0 → D4 Bit 1 → D5 Bit 2 → D8 Bit 3 → D10 Bit 5 → D17 Bit 6 → D20	1200	1200	NA
07	15	SPD	Store PSR Designators	PSR D-bits $\rightarrow U_{6-0}$; D4 → Bit 0 D5 → Bit 1 D8 → Bit 2 D10 → Bit 3 D12 → Bit 4 D17 → Bit 5 D20 → Bit 6	300	300	NA
07	16	LBR (a=0)	Load Breakpoint Register	(U) → Breakpoint Register	1500	1500	NA
07	16	SJS (a=1)	Store Jump Stack	(Jump History Stack) → U through U+3 *NOTE:* *The SJS instruction is noninterruptible*	1200	1200	NA
07	17	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	3800	3800	NA
10	0–17	L, LA	Load A	(U) → A	300	440	NA
11	0–17	LN, LNA	Load Negative A	–(U) → A	300	440	NA
12	0–17	LM, LMA	Load Magnitude A	$\lvert(U)\rvert \rightarrow A$	300	440	NA
13	0–17	LNM, LNMA	Load Negative Magnitude A	$-\lvert(U)\rvert \rightarrow A$	300	440	NA

**See Appendix A for notational conventions.*
†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
14	0–17	A, AA	Add To A	(A)+(U) → A	300	440	NA
15	0–17	AN, ANA	Add Negative To A	(A) – (U) → A	300	440	NA
16	0–17	AM, AMA	Add Magnitude To A	$(A)+\lvert(U)\rvert \rightarrow A$	300	440	NA
17	0–17	ANM, ANMA	Add Negative Magnitude To A	$(A)-\lvert(U)\rvert \rightarrow A$	300	440	NA
20	0–17	AU	Add Upper	(A)+(U) → A+1	300	440	NA
21	0–17	ANU	Add Negative Upper	(A)–(U) → A+1	300	440	NA
22	0–15	BT	Block Transfer, Repeat	$(X_x+u) \rightarrow X_a+u$; repeat K times	900K	1480K	1040
23	0–17	L, LR	Load R	$(U) \rightarrow R_a$	300	440	NA
24	0–17	A, AX	Add To X	$(X_a)+(U) \rightarrow X_a$	300	440	NA
25	0–17	AN, ANX	Add Negative To X	$(X_a)-(U) \rightarrow X_a$	300	440	NA
26	0–17	LXM	Load X Modifier	$(U) \rightarrow X_{a_{17-0}}; X_{a_{35-18}}$ unchanged	300	440	NA
27	0–17	L, LX	Load X	$(U) \rightarrow X_a$	300	440	NA
30	0–17	MI	Multiply Integer	(A)•(U) → A,A+1	1500	1500	NA
31	0–17	MSI	Multiply Single Integer	(A)•(U) → A	1500	1500	NA
32	0–17	MF	Multiply Fractional	(A)•(U) → A,A+1	1500	1500	NA
33	00	BM	Byte Move	Transfer N bytes from source string to receiving string. Truncate or fill receiving string as required	2120	NA	2100
33	01	BMT	Byte Move With Translate	Translate and transfer N bytes from source string to receiving string. Truncate or fill receiving string as required	3320	NA	2100
33	02	BTT	Byte Translate and Test	Translate and test N bytes against (A); if not equal; terminate instruction with J0 pointing to unequal byte and N≠0	2860	NA	2100
33	03	BTC	Byte Translate and Compare	Translate and compare N bytes from string E to M bytes from string F; terminate instruction on not equal or when both M and N have been reduced to zero; when: (A)>0; string E>F (A)=0; string E=F (A)<0; string E<F	4520	NA	2100
33	04	BC	Byte Compare	Compare N bytes from string E to M bytes from string F; terminate instruction on not equal or when both M and N are zero	2120	NA	2100

**See Appendix A for notational conventions.*

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
33	05	BPD	Byte to Packed Decimal Convert	Convert N bytes in string E to packed decimal in string F	1590	NA	4220
33	06	PDB	Packed Decimal to Byte Convert	Convert N packed decimal digits in string E to bytes in string F	1590	NA	4220
33	07	EDIT	Edit	Edit byte string E and transfer to byte string F under the control of string G (see Note 4 (b))			8480
				Skip	2120+ $740K_1$	NA	
				Editing action	3640+ $2280K_2$	NA	
				Blank if zero	300 $+740K_2$	NA	
33	10	BI	Byte to Binary Single Integer Convert	Convert N bytes in string E into a signed binary integer in register A	8960	NA	2700
33	11	BDI	Byte to Binary Double Integer Convert	Convert N bytes in string E into a signed binary integer in registers A and A+1	14580	NA	2700
33	12	IB	Binary Single Integer to Byte Convert	Convert the binary integer in A to byte format and store in string E	15600	NA	8700
33	13	DIB	Binary Double Integer to Byte Convert	Convert the binary integer in A and A+1 to byte format and store in string E	30260	NA	15300
33	14	BF	Byte to Single Floating Convert	Convert N bytes in string E into a single length floating point format in register A	See Note 10	NA	See Note 10
33	15	BDF	Byte to Double Floating Convert	Convert N bytes in string E into a double length floating point format in registers A, A+1	See Note 10	NA	See Note 10
33	16	FB	Single Floating to Byte Convert	Convert the single length floating point number in A to byte format and store in string E	61590	NA	2700
33	17	DFB	Double Floating to Byte Convert	Convert the double length floating point number in A and A+1 to byte format and store in string E	70190	NA	2700
34	0–17	DI	Divide Integer	(A, A+1)÷(U) → A; REMAINDER → A+1	6400	6400	NA
35	0–17	DSF	Divide Single Fractional	(A)÷(U) → A+1	6400	6400	NA
36	0–17	DF	Divide Fractional	(A, A+1)÷(U) → A; REMAINDER → A+1	6400	6400	NA
37	00	QB	Quarter-Word Byte to Binary Compress	Discard $(A)_{35}$, $(A)_{26}$, $(A)_{17}$, and $(A)_8$; place the remaining bits in A_{31-0}; $(A)_{31} \rightarrow A_{35-32}$	300	NA	NA
37	01	BQ	Binary to Quarter-Word Byte Extend	Discard $(A)_{35-32}$; place the remaining bits in A_{34-27}, A_{25-18}, A_{16-9}, and A_{7-0}; zero fill A_{35}, A_{26}, A_{17}, and A_8	300	NA	NA

**See Appendix A for notational conventions.*

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
37	02	QBH	Quarter-Word Byte to Binary Halves Compress	Discard $(A)_{35}$, $(A)_{26}$, $(A)_{17}$, and $(A)_8$; place the remaining bits in A_{33-18} and A_{15-0}; $(A)_{33}$ → A_{35-34}; $(A)_{15}$→A_{17-16}	300	NA	NA
37	03	BHQ	Binary Halves to Quarter-Word Byte Extend	Discard $(A)_{35-34}$ and $(A)_{17-16}$; place the remaining bits in A_{34-27}, A_{25-18}, A_{16-9}, and A_{7-0}; zero fill A_{35}, A_{26}, A_{17}, and A_8	300	NA	NA
37	04	QDB	Quarter-Word Byte to Double Binary Compress	Discard A_{35}, A_{26}, A_{17}, A_8, $A{+}1_{35}$, $A{+}1_{26}$, $A{+}1_{17}$, and $A{+}1_8$; place the remaining bits in A_{27-0} and A+1; $(A)_{27}$ → A_{35-28}	300	NA	NA
37	05	DBQ	Double Binary to Quarter-Word Byte Extend	Discard $(A)_{35-28}$; place the remaining bits from A and A+1 in A_{34-27}, A_{25-18}, A_{16-9}, A_{7-0}, $A{+}1_{34-27}$, $A{+}1_{25-18}$, $A{+}1_{16-9}$, and $A{+}1_{7-0}$; zero fill A_{35}, A_{26}, A_{17}, A_8, $A{+}1_{35}$, $A{+}1_{26}$, $A{+}1_{17}$, and $A{+}1_8$	300	NA	NA
37	06	BA	Byte Add	Add the N bytes in string E to the M bytes in string F and place the result in string G	3180 (sign correct) 5600 (sign incorrect)	NA NA	2100 2400
37	07	BAN	Byte Add Negative	Subtract the N bytes in string E from the M bytes in string F and place the result in string G	3180 (sign correct) 5600 (sign incorrect)	NA NA	2100 2400
37	10–17	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	3800	3800	NA
40	0–17	OR	Logical OR	(A) OR (U) → A+1	300	440	NA
41	0–17	XOR	Logical Exclusive OR	(A) XOR (U) → A+1	300	440	NA
42	0–17	AND	Logical AND	(A) AND (U) → A+1	300	440	NA
43	0–17	MLU	Masked Load Upper	[(U) AND (R2)] OR [(A) AND (R2)′] → A+1	440	1640	NA
44	0–17	TEP	Test Even Parity	Skip NI if (U) AND (A) has even parity	1500/ 1200	1640/ 1340	NA
45	0–17	TOP	Test Odd Parity	Skip NI if (U) AND (A) has odd parity	1500/ 1200	1640/ 1440	NA
46	0–17	LXI	Load X Increment	(U) → $(X_a)_{35-18}$; $(X_a)_{17-0}$ unchanged	300	440	NA
47	0–17	TLEM	Test Less Than or Equal to Modifier	Skip NI if $(U) \leqslant (X_a)_{17-0}$; always $(X_a)_{17-0}+(X_a)_{35-18} \rightarrow X_{a_{17-0}}$	1500/ 1200	1640/ 1340	NA
		TNGM	Test Not Greater Than Modifier				
50	0–17	TZ	Test Zero	Skip NI if (U)=±0	1500/ 1200	1640/ 1340	NA

**See Appendix A for notational conventions.*
†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
51	0–17	TNZ	Test Nonzero	Skip NI if $(U)\neq\pm0$	1500/ 1200	1640/ 1340	NA
52	0–17	TE	Test Equal	Skip NI if $(U)=(A)$	1500/ 1200	1640/ 1340	NA
53	0–17	TNE	Test Not Equal	Skip NI if $(U)\neq(A)$	1500/ 1200	1640/ 1340	NA
54	0–17	TLE	Test Less Than or Equal	Skip NI if $(U)\leqslant(A)$	1500/ 1200	1640/ 1340	NA
		TNG	Test Not Greater				
55	0–17	TG	Test Greater	Skip NI if $(U)>(A)$	1500/ 1200	1640/ 1340	NA
56	0–17	TW	Test Within Range	Skip NI if $(A)<(U)\leqslant(A+1)$	1500/ 1200	1640/ 1340	NA
57	0–17	TNW	Test Not Within Range	Skip NI if $(U)\leqslant(A)$ or $(U)>(A+1)$	1500/ 1200	1640/ 1340	NA
60	0–17	TP	Test Positive	Skip NI if $(U)_{35}=0$	1500/ 1200	1640/ 1340	NA
61	0–17	TN	Test Negative	Skip NI if $(U)_{35}=1$	1500/ 1200	1640/ 1340	NA
62	0–17	SE	Search Equal	Skip NI if $(U)=(A)$, else repeat	750K	740K	1190
63	0–17	SNE	Search Not Equal	Skip NI if $(U)\neq(A)$, else repeat	750K	740K	1190
64	0–17	SLE	Search Less Than or Equal	Skip NI if $(U)\leqslant(A)$, else repeat repeat	750K	740K	1190
		SNG	Search Not Greater				
65	0–17	SG	Search Greater	Skip NI if $(U)>(A)$, else repeat	750K	740K	1190
66	0–17	SW	Search Within Range	Skip NI if $(A)<(U)\leqslant(A+1)$, else repeat	750K	740K	1190
67	0–17	SNW	Search Not Within Range	Skip NI if $(U)\leqslant(A)$ or $(U)>(A+1)$, else repeat	750K	740K	1190
70	0–17	JGD	Jump Greater and Decrement	Jump to U if (Control Register$_{ja}$) >0; go to NI if (Control Register$_{ja}$) $\leqslant0$; always (Control Register$_{ja}$) $-1\rightarrow$ Control Register$_{ja}$	830/ 350	830/ 350	NA
71	00	MSE	Mask Search Equal	Skip NI if (U) AND (R2) = (A) AND (R2), else repeat	750K	750K	1190
71	01	MSNE	Mask Search Not Equal	Skip NI IF (U) AND (R2) ≠(A) AND (R2), else repeat	750K	750K	1190
71	02	MSLE	Mask Search Less Than or Equal	Skip NI if (U) AND (R2) ≤ (A) AND (R2), else repeat	750K	750K	1190
		MSNG	Mask Search Not Greater				

*See Appendix A for notational conventions.
†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
71	03	MSG	Mask Search Greater	Skip NI if (U) AND (R2) > (A) AND (R2), else repeat	750K	750K	1190
71	04	MSW	Masked Search Within Range	Skip NI if (A) AND (R2)<(U) AND (R2)≤(A+1) AND (R2), else repeat	750K	750K	1190
71	05	MSNW	Masked Search Not Within Range	Skip NI if (U) AND (R2)≤(A) AND (R2) or (U) AND (R2)>(A+1) AND (R2), else repeat	750K	750K	1190
71	06	MASL	Masked Alphanumeric Search Less Than or Equal	Skip NI if (U) AND (R2)≤(A) AND (R2), else repeat	750K	750K	1190
71	07	MASG	Masked Alphanumeric Search Greater	Skip NI if (U) AND (R2)>(A) AND (R2), else repeat	750K	750K	1190
71	10	DA	Double Precision Fixed-point Add	(A, A+1) + (U, U+1) → A, A+1	600	600	NA
71	11	DAN	Double Precision Fixed-Point Add Negative	(A, A+1) – (U, U+1) → A, A+1	600	600	NA
71	12	DS	Double Store A	(A, A+1) → U, U+1	600	600	NA
71	13	DL	Double Load A	(U, U+1) → A, A+1	600	600	NA
71	14	DLN	Double Load Negative A	–(U, U+1) → A, A+1	600	600	NA
71	15	DLM	Double Load Magnitude A	|(U, U+1)| → A, A+1	600	600	NA
71	16	DJZ	Double Precision Jump Zero	Jump to U if (A, A+1) = ±0; go to NI if (A, A+1) ≠ ±0	830/ 350	830/ 350	NA
71	17	DTE	Double Precision Test Equal	Skip NI if (U, U+1) = (A, A+1)	1800/ 1500	1800/ 1500	NA
72	00	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	3800	3800	NA
72	01	SLJ	Store Location and Jump	(P) – BASE ADDRESS MODIFIER [BIX/BI or BDX/BD] → U_{17-0}; jump to U+1	1430	1430	NA
72	02	JPS	Jump Positive and Shift	Jump to U if $(A)_{35}=0$; go to NI if $(A)_{35}=1$; always shift (A) left circularly one bit position	830/ 350	830/ 350	NA
72	03	JNS	Jump Negative and Shift	Jump to U if $(A)_{35}=1$; go to NI if $(A)_{35}=0$; always shift (A) left circularly one bit position	830/ 350	830/ 350	NA
72	04	AH	Add Halves	$(A)_{35-18}+(U)_{35-18} \rightarrow (A)_{35-18}$; $(A)_{17-0}+(U)_{17-0} \rightarrow A_{17-0}$	300	300	NA
72	05	ANH	Add Negative Halves	$(A)_{35-18}-(U)_{35-18} \rightarrow (A)_{35-18}$; $(A)_{17-0}-(U)_{17-0} \rightarrow A_{17-0}$	300	300	NA

**See Appendix A for notational conventions.*

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
72	06	AT	Add Thirds	$(A)_{35-24}+(U)_{35-24} \rightarrow A_{35-24}$; $(A)_{23-12}+(U)_{23-12} \rightarrow A_{23-12}$; $(A)_{11-0}+(U)_{11-0} \rightarrow A_{11-0}$	300	300	NA
72	07	ANT	Add Negative Thirds	$(A)_{35-24}-(U)_{35-24} \rightarrow A_{35-24}$; $(A)_{23-12}-(U)_{23-12} \rightarrow A_{23-12}$; $(A)_{11-0}-(U)_{11-0} \rightarrow A_{11-0}$	300	300	NA
72	10	EX	Execute	Execute the instruction at U	830	830	NA
72	11	ER	Executive Return	Causes executive return interrupt to address 242_8	3830	3830	NA
72	12	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	3800	3800	NA
72	13	PAIJ	Prevent All I/O Interrupts and Jump	Prevent all I/O interrupts and jump to U	830	830	NA
72	14	SCN	Store Channel Number	If a=0, number of the interrupting I/O channel → U_{3-0} If a=1, number of the interrupting I/O channel → U_{3-0}; CAU number → U_{5-4} If a=2, number of the interrupting I/O channel → U_{5-0} If a=3, number of the interrupting I/O channel → U_{5-0}; CAU number → U_{14-12}	300	300	NA
72	15	LPS (a=0)	Load Processor State Register	(U) → PSRM	1500	1500	NA
72	15	LMP (a=1)	Load Main Processor State Register	(U, U+1) → PSRM, PSRME	1500	1500	NA
72	15	LUP (a=2)	Load Utility Processor State Register	(U, U+1) → PSRU, PSRUE	1500	1500	NA
72	16	LSL (a=0)	Load Main Storage Limits Register	(U) → SLRM	1500	1500	NA
72	16	LUS (a=1)	Load Utility Storage Limits Register	(U) → SLRU	1500	1500	NA
72	16	SL (a=2)	Store Main Storage Limits Register	(SLRM) → U	300	300	NA
72	16	SUL (a=3)	Store Utility Storage Limits Register	(SLRU) → U	300	300	NA
72	17	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	3800	3800	NA
73	00	SSC	Single Shift Circular	Shift (A) right circularly U places	300	300	NA

**See Appendix A for notational conventions.*

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
73	01	DSC	Double Shift Circular	Shift (A, A+1) right circularly U places	300	300	NA
73	02	SSL	Single Shift Logical	Shift (A) right U places; zerofill	300	300	NA
73	03	DSL	Double Shift Logical	Shift (A, A+1) right U places; zerofill	300	300	NA
73	04	SSA	Single Shift Algebraic	Shift (A) right U places; signfill	300	300	NA
73	05	DSA	Double Shift Algebraic	Shift (A, A+1) right U places; signfill	300	300	NA
73	06	LSC	Load Shift and Count	(U) → A, shift (A) left circularly until $(A)_{35} \neq (A)_{34}$; NUMBER OF SHIFTS → A+1	400	400	NA
73	07	DLSC	Double Load Shift and Count	(U, U+1) → A, A+1; shift (A, A+1) left circularly until $(A, A+1)_{71} \neq (A, A+1)_{70}$; NUMBER OF SHIFTS → A+2	2100	2100	NA
73	10	LSSC	Left Single Shift Circular	Shift (A) left circularly U places	300	300	NA
73	11	LDSC	Left Double Shift Circular	Shift (A, A+1) left circularly U places	300	300	NA
73	12	LSSL	Left Single Shift Logical	Shirt (A) left U places; zerofill	300	300	NA
73	13	LDSL	Left Double Shift Logical	Shift (A, A+1) left U places; zerofill	300	300	NA
73	14	III (a=0 through 3)	Initiate Interprocessor-Interrupt	Initiate Interprocessor-interrupt per a: a=0: Interrupt CAU Number 0 a=1: Interrupt CAU Number 1 a=2: Interrupt CAU Number 2 a=3: Interrupt CAU Number 3	300	300	NA
73	14	EDC $(a=11_8)$	Enable Day Clock	Enable day clock	300	300	NA
73	14	DDC $(a=12_8)$	Disable Day Clock	Disable day clock	300	300	NA
73	14	CES $(a=13_8)$	Clear and Enable Storage Reference Counters	Clear storage reference counters to zero and enable on NI	300	300	NA
73	14	ES $(a=14_8)$	Enable Storage Reference Counters	Enable storage reference counters on NI and carry values from last interrupt forward	300	300	NA
73	15	SIL	Select Interrupt Locations	$(U)_{8-0}$ → MSR	1200	1200	NA

**See Appendix A for notational conventions.*

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
73	16	LCR (a=0)	Load Channel Select Register	$(U)_{5-0}$ → CSR; if $(U)_9$=1, condition channel for back-to-back data transfer	1200	1200	NA
		LLA (a=1)	Load Last Address Register	$(U)_{8-0}$ → LAR	1200	1200	NA
73	17	TS (a=0)	Test and Set	If $(U)_{30}$=1, interrupt; if $(U)_{30}$=0, go to NI. Always set $(U)_{35-30}$ to 01_8	5030/ 1200	5030/ 1200	NA
73	17	TSS (a=1)	Test and Set and Skip	If $(U)_{30}$=0, skip; if $(U)_{30}$=1, go to NI. Always set $(U)_{35-30}$ to 01_8	1500/ 1200	1500/ 1200	NA
73	17	TCS (a=2)	Test and Clear and Skip	If $(U)_{30}$=0, go to NI; if $(U)_{30}$=1, skip. Always clear $(U)_{35-30}$	1500/ 1200	1500/ 1200	NA
74	00	JZ	Jump Zero	Jump to U if (A) = ± 0; go to NI if $(A) \neq \pm 0$	830/ 350	830/ 350	NA
74	01	JNZ	Jump Nonzero	Jump to U if $(A) \neq \pm 0$; go to NI if (A) = ±0	830/ 350	830/ 350	NA
74	02	JP	Jump Positive	Jump to U if $(A)_{35}$=0; go to NI if $(A)_{35}$=1	830/ 350	830/ 350	NA
74	03	JN	Jump Negative	Jump to U if $(A)_{35}$=1; go to NI if $(A)_{35}$=0	830/ 350	830/ 350	NA
74	04	JK J	Jump Keys Jump	Jump to U if a=0 or if a=lit select jump indicator; go to NI if neither is true	830/ 350	830/ 350	NA
74	05	HKJ HJ	Halt Keys and Jump Halt Jump	Stop if a=0 or if [a AND lit select stop indicators] ≠ 0; on restart or continuation, jump to U	830	830	NA
74	06	NOP	No Operation	Proceed to NI	300	300	NA
74	07	AAIJ	Allow All I/O Interrupts and Jump	Allow all I/O interrupts and jump to U	830	830	NA
74	10	JNB	Jump No Low Bit	Jump to U if $(A)_0$=0; go to NI if $(A)_0$=1	830/ 350	830/ 350	NA
74	11	JB	Jump Low Bit	Jump to U if $(A)_0$=1; go to NI if $(A)_0$=0	830/ 350	830/ 350	NA
74	12	JMGI	Jump Modifier Greater and Increment	Jump to U if $(X_a)_{17-0}>0$; go to NI if $(X_a)_{17-0}\leq 0$; always $(X_a)_{17-0}+(X_a)_{35-0} \rightarrow X_{a_{17-0}}$	830/ 350	830/ 350	NA
74	13	LMJ	Load Modifier and Jump	(P) – BASE ADDRESS MODIFIER [BIX/BI or BDX/BD] → $(X_a)_{17-0}$; jump to U	830	830	NA

*See Appendix A for notational conventions.

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
74	14	JO (a=0)	Jump Overflow	Jump to U if D1 of PSR=1; go to NI if D1=0	830/350	830/350	NA
74	14	JFU (a=1)	Jump Floating Underflow	Jump to U if D21 of PSR=1; go to NI if D21=0; clear D21	830/350	830/350	NA
74	14	JFO (a=2)	Jump Floating Overflow	Jump to U if D22 of PSR=1; go to NI if D22=0; clear D22	830/350	830/350	NA
74	14	JDF (a=3)	Jump Divide Fault	Jump to U if D23 of PSR=1; go to NI if D23=0; clear D23	830/350	830/350	NA
74	15	JNO (a=0)	Jump No Overflow	Jump to U if D1 of PSR=0; go to NI if D1=1	830/350	830/350	NA
74	15	JNFU (a=1)	Jump No Floating Underflow	Jump to U if D21 of PSR=0; go to NI if D21=1; clear D21	830/350	830/350	NA
74	15	JNFO (a=2)	Jump No Floating Overflow	Jump to U if D22 of PSR=0; go to NI if D22=1; clear D22	830/350	830/350	NA
74	15	JNDF (a=3)	Jump No Divide Fault	Jump to U if D23 of PSR=0; go to NI if D23=1; clear D23	830/350	830/350	NA
74	16	JC	Jump Carry	Jump to U if D0 of PSR=1; go to NI if D0=0	830/350	830/350	NA
74	17	JNC	Jump No Carry	Jump to U if D0 of PSR=0; go to NI if D0=1	830/350	830/350	NA
75	00	LIC	Load Input Channel	For channel [a OR CSR]; (U) → IACR; set input active; clear input monitor	600	600	NA
75	01	LICM	Load Input Channel and Monitor	For channel [a OR CSR]; (U) → IACR; set input active; set input monitor	600	600	NA
75	02	JIC	Jump on Input Channel Busy	Jump to U if input active is set for channel [a OR CSR]; go to NI if input active is clear	1130/650	1130/650	NA
75	03	DIC	Disconnect Input Channel	For channel [a OR CSR]; clear input active; clear input monitor	600	600	NA
75	04	LOC	Load Output Channel	For channel [a OR CSR]; (U) → OACR; set output active; clear output monitor; clear external function (ISI only)	600	600	NA
75	05	LOCM	Load Output Channel and Monitor	For channel [a OR CSR]; (U) → OACR; set output active; set output monitor; clear external function (ISI only)	600	600	NA
75	06	JOC	Jump on Output Channel Busy	Jump to U if output active is set for channel [a OR CSR]; go to NI if output active is clear	1130/650	1130/650	NA

**See Appendix A for notational conventions.*

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
75	07	DOC	Disconnect Output Channel	For channel [a OR CSR]; clear output active; clear output monitor; clear external function	600	600	NA
75	10	LFC	Load Function in Channel	For channel [a OR CSR]; (U) → OACR; set output active (ISI only), external function, and force external function; clear output monitor (ISI only)	600	600	NA
75	11	LFCM	Load Function in Channel and Monitor	For channel [a OR CSR]; (U) → OACR; set output active (ISI only), external function, force external function, and output monitor (ISI only)	600	600	NA
75	12	JFC	Jump on Function in Channel	Jump to U if force external function is set for channel [a OR CSR]; go to NI if force external function is clear	1130/ 650	1130/ 650	NA
75	14	AACI	Allow All Channel External Interrupts	Allow all channel external interrupts	600	600	NA
75	15	PACI	Prevent All Channel External Interrupts	Prevent all channel external interrupts	600	600	NA
75	16	ACI	Allow Channel Interrupts	If a=0, allow interrupts on channels 23–0 specified by 1 bits in $(U)_{23-0}$ If a=1, allow interrupts on channels 47–24 specified by 1 bits in $(U)_{23-0}$	600	600	NA
75	17	PCI	Prevent Channel Interrupts	If a=0, prevent interrupts on channels 23–0 specified by 1 bits in $(U)_{23-0}$ If a=1, prevent interrupts on channels 47–24 specified by 1 bits in $(U)_{23-0}$	600	600	NA
76	00	FA	Floating Add	(A)+(U) → A; RESIDUE → A+1 if D17=1	900**	900**	NA
76	01	FAN	Floating Add Negative	(A)–(U) → A; RESIDUE → A+1 if D17=1	900**	900**	NA
76	02	FM	Floating Multiply	(A)·(U) → A (and A+1 if D17=1)	1650	1650	NA
76	03	FD	Floating Divide	(A)÷(U) → A; REMAINDER → A+1 if D17=1	5300	5300	NA
76	04	LUF	Load and Unpack Floating	$\|(U)\|_{34-27} \rightarrow A_{7-0}$, zerofill; $(U)_{26-0} \rightarrow A+1_{26-0}$, signfill	350	350	NA

*See Appendix A for notational conventions.

**Minus 140 nanoseconds if D17 is clear.

†See Notes at end of table for additional information on instruction timing.

Function Code (Octal)		Mnemonic	Instruction	Description*	Instruction Time (in nsecs)†		
f	j				1	2	3
76	05	LCF	Load and Convert to Floating	$(U)_{35} \rightarrow A+1_{35}$, [NORMALIZED $(U)]_{26-0} \rightarrow A+1_{26-0}$; if $(U)_{35}=0$, $(A)_{7-0} \pm$ NORMALIZING COUNT → $A+1_{34-27}$; if $(U)_{35}=1$, ones complement of $[(A)_{7-0} \pm$ NORMALIZING COUNT] → $A+1_{34-27}$	750	750	NA
76	06	MCDU	Magnitude of Characteristic Difference to Upper	$\lvert\lvert(A)\rvert_{35-27} - \lvert(U)\rvert_{35-27}\rvert \rightarrow (A+1)_{8-0}$; ZEROS → $A+1_{35-9}$	300	300	NA
76	07	CDU	Characteristic Difference to Upper	$\lvert(A)\rvert_{35-27} - \lvert(U)\rvert_{35-27} \rightarrow A+1_{8-0}$; SIGN BITS → $A+1_{35-9}$	300	300	NA
76	10	DFA	Double Precision Floating Add	(A, A+1) + (U, U+1) → A, A+1	750	750	NA
76	11	DFAN	Double Precision Floating Add Negative	(A, A+1) – (U, U+1) → A, A+1	750	750	NA
76	12	DFM	Double Precision Floating Multiply	(A, A+1) · (U, U+1) → A, A+1	2400	2400	NA
76	13	DFD	Double Precision Floating Divide	(A, A+1) ÷ (U, U+1) → A, A+1	10300	10300	NA
76	14	DFU	Double Load and Unpack Floating	$\lvert(U,U+1)_{70-60}\rvert \rightarrow A_{10-0}$, zerofill; $(U,U+1)_{59-36} \rightarrow A+1_{23-0}$, signfill; $(U,U+1)_{35-0} \rightarrow A+2$	2100	2100	NA
76	15	DLCF, DFP	Double Load and Convert to Floating	$(U)_{35} \rightarrow A+1_{35}$; [NORMALIZED $(U, U+1)]_{59-0} \rightarrow A+1_{23-0}$ and A+2; If $(U)_{35}=0$, $(A)_{10-0} \pm$ NORMALIZING COUNT → $A+1_{34-24}$; If $(U)_{35}=1$, ones complement of $[(A)_{10-0} \pm$NORMALIZING COUNT] → $A+1_{34-24}$	2400	2400	NA
76	16	FEL	Floating Expand and Load	$(U)_{26-3} \rightarrow A_{23-0}$; $(U)_{2-0} \rightarrow A+1_{35-33}$; $(U)_{35} \rightarrow A+1_{32-0}$; If $(U)_{35}=0$, $(U)_{35-27} + 1600_8 \rightarrow A_{35-24}$; if $(U)35=1$, $(U)_{35-27} - 1600_8 \rightarrow A_{35-24}$	300	300	NA
76	17	FCL	Floating Compress and Load	$(U)_{23-0} \rightarrow A_{26-3}$; $(U+1)_{35-33} \rightarrow A_{2-0}$; if $(U)_{35}=0$, $(U)_{35-24} - 1600_8 \rightarrow A_{35-27}$; if $(U)_{35}=1$, $(U)_{35-24} + 1600 \rightarrow A_{35-27}$	600	600	NA
77	0–17	–	Invalid Code	Causes invalid instruction interrupt to address 241_8	3800	3800	NA

*See Appendix A for notational conventions.

†See Notes at end of table for additional information on instruction timing.

NOTES:

1. The instruction times are estimated with no conflicts in storage and optimized timing between control, arithmetic, storage spigots, GRS, and IOAU.

2. The timing estimations used only whole word stores with the exception of the byte instructions which must use partial stores.

3. Instruction timing is as follows (see note 5):

   Column 1: Primary Storage

   Column 2: Primary Storage (with character addressing).

4. Repeated Instructions

   Repeated instruction times can be estimated by these formulas:

   (a) Total time = set up + number of repeats x basic times (K).

   (b) Edit in the byte instruction is estimated by K_1 = skip count, K_2 = number of control bytes.

5. Instruction set up times are special sequences to condition the control for repeated sequences and are added to the total time required for the repeated instruction.

   Column 3: Primary Storage set-up time.

6. Test or skip instruction times are stated as 1500/1200. The first number is the time for skip taken and the second is for skip not taken.

7. Conditional jump times are stated as 830/350. The first number is time for jump taken, the second for jump not taken.

8. Instruction times are calculated from timing charts and can vary up to ± 5% with the exception of 07–14, 15; 37–06,07 and all 33 instructions, which may vary ± 20% because they are data dependent. IOAU instructions must be spaced at least five instructions apart to obtain maximum rate.

9. Added Sequences

   (a) Auto Mode

   When the CAU is in the auto mode (PSR D18 set) and a limit error occurs during operand address generation, 300 nanoseconds must be added to the instruction time.

   When doing character addressing (PSR D4 set) or byte instructions auto mode cannot occur.

   (b) Indirect Addressing

   The control is conditioned for indirect addressing when D7 and D11 are equal to 0 and the i field of the instruction word is equal to 1. The indirect addressing adds 830 nanoseconds to the instruction time in columns 1 and 2, and 1750 nanoseconds in column 3.

   (c) Operand Basing

   When the control is conditioned for operand basing by D11 set and i-bit set in the instruction word, 300 nanoseconds are added to the instruction time.

   (d) X Overflow

   When the index registers overflow on the 262K wrap around, another address must be generated, therefore, adding another 300 nanoseconds to the instruction time.

10. Execution Times for Byte to Floating Conversions (33—14, 15) Instructions

(a) Time for special case of no exponent field, no decimal point, and BB1 = 0:

$$\begin{aligned} T_{\text{special}}(\text{nsec.}) &= 300\cdot A+300\cdot B+1060\cdot C+300\cdot D \\ &\quad +300\cdot E+300\cdot F+380+650N \\ &\quad +PQR \\ &= 300(A+B+D+E+F)+1060\cdot C+650N+380 \\ &\quad +PQR \end{aligned}$$

(b) Time for non-special case:

$$\begin{aligned} T_{\text{total}}(\text{nsec.}) &= T_{\text{special}}+180+210\cdot G+180+490\cdot H+670 \\ &\quad +390+12(180)+640+2200\cdot K+300 \\ &\quad +2200\cdot L+300+180+2200\cdot M+10{,}100(1-M) \\ &= 210\cdot G+490\cdot H+2200\cdot(K+L+M) \\ &\quad +10{,}100(1-M)+5000+T_{\text{special}} \end{aligned}$$

Where:

A = number of leading blanks.
B = 1 if mantissa sign present, 0 otherwise.
C = number of digits or significant blanks in mantissa.
D = 1 if decimal point present, 0 otherwise.
E = 1 if D or E present, 0 otherwise.
F = 1 if exponent sign field present, 0 otherwise.
G = number of blanks after mantissa but before exponent or exponent sign.
H = number of digits or significant blanks in exponent field.
K = 1 if $D3 \neq 0$ and $D2 \neq 0$ in corrected exponent, 0 otherwise.
L = 1 if $D1 \neq 0$ and, either $D2 \neq 0$ or $D3 \neq 0$, 0 otherwise.
M = 1 if corrected exponent $\geqslant 0$, 0 otherwise.
N = 1 if 33—14 instruction, 0 if 33—15 instruction.
P = number of bytes.
Q = fetch time of bytes is 720 nanoseconds.
R = estimated 50% of fetch time hidden by execution cycle $0 \leqslant R \leqslant 1$.