Marinchip Systems M9900 CPU

Compatibility Bulletin

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1. Introduction

This document is a continually-expanding collection of information about compatibility between the M9900 CPU and other boards which operate on the S-100 bus. Since the S-100 bus is not a strict standard, and many boards were designed with a specific application in mind, it cannot be assumed that any board called "S-100 compatible" will work with any other unless the design is carefully examined, or experience has shown the two to work together. This bulletin is divided into classes of boards, and discusses specific information and experience with various boards. The comments made about various components are the result of our experience using those components at Marinchip Systems. Other users may have had different experience (for example, we may have gotten a lemon, or conversely, the only one that worked), so we are always interested in hearing your experiences. In particular, please let us know about your experience using components not included in this Bulletin: the more things we can include, the easier it will be to configure systems.

1.1. General compatibility considerations

Several general statements may be made about which boards will and will not work with the M9900 CPU. In general, almost any static memory, or any non-timing-critical I/O board which uses 8080 IN and OUT instructions for its I/O will work with no trouble. Dynamic memory boards will work fine, unless they count on the specific pattern of memory cycles generated by an 8080 or Z-80 to control their refresh. Be careful when selecting dynamic memory to make sure it will work with any DMA devices in your system (such as disc controllers) as well as with the M9900 CPU. I/O boards which use memory-mapped I/O may cause troubles, since the M9900 CPU always accesses two bytes in sequence. If this causes trouble in accessing the board, it may not be usable. Boards which count on the 8080 quirk of placing the status lines on the data bus during the SYNC cycle will not work, but fortunately these boards are very rare and can usually be easily modified to correct this problem. The M9900, if running with all 8-bit memory, cannot execute a tight loop as fast as an 8080 (because the minimum instruction length on the 9900 is 16 bits). This can cause trouble with boards that require very tight timing loops (such as non-DMA disc controllers). These boards may be run by the appropriate use of Marinchip 16-bit memory boards in the system.

This section has tried to list all the compatibility problems known. Do not be discouraged: most peripherals are designed very

well, and will run with no trouble.

2. Memory Boards

2.1. Static memory

2.1.1. Processor Technology 8KRA

Works fine. This board is no longer manufactured.

2.1.2. Industrial Micro Systems 8K

Works fine.

2.1.3. Vector Graphic 8K

Works fine.

2.1.4. Industrial Micro Systems 16K

Works fine. This is a prince of a memory board: it has bank selection to permit addressing up to 4 MEGABYTES, phantom line disable, and the ability to lock out any 1K area to fit around a boot PROM.

2.1.5. Artec Electronics 32K

Works fine. You can order this in 8K multiples from 8 to 32K.

2.1.6. Seattle Computer Products 16K

Works fine. This is their model 24-101. We have tested only the 250 ns version of this board, but the 450 ns version should work as well since it differs only in the speed of the chips and 450 ns is fast enough for the M9900 CPU.

2.1.7. Problem Solver Systems RAM 16

Works fine.

2.1.8. Thinker Toys SuperRam 16K

Works fine.

2.1.9. Godbout Econoram II 8K

This board is a very old design which implements the memory protect feature used in the original Altair 8800 (where it all began). The memory protect line is not used on modern S-100 systems, and if left floating, this board will work erratically. If you are using this board, you should jumper pin 70 of the bus to ground (you can do this on the 8K board itself). With this change, the board works fine. Note that these comments apply only to the original 8K Godbout, not the redesigned version which used 4K RAM chips instead of the original 1K chips.

2.1.10. Godbout Econoram IV 16K

Works fine.

2.1.11. Godbout Econoram VII 24K

Works fine.

2.1.12. WAMECO MEM-2 16K

Works fine.

2.1.13. California Computer Systems 16K

Works fine.

2.1.14. Digital Research of Texas 16K

Works fine.

2.2. Dynamic memory

2.2.1. Marinchip M9900 64K

This board is a 64K byte RAM board designed explicitly to run with the M9900 CPU, and is sold assembled and tested by Marinchip Systems and our dealers. Unlike conventional S-100 bus boards, this board takes advantage of the M9900 CPU's 16 bit mode, so data is transferred between the CPU and RAM 16 bits at a time, rather than in pairs of 8 bit accesses. This, and the unique fast cycle timing of the RAM board, triples memory bandwidth, which generally results in halving the execution time of CPU bound programs. The RAM board permits bank selection in 4K byte blocks. The initial bank selection of a board is set by DIP switches, and may be subsequently altered by I/O to a 16 bit wide I/O port contained on the board. Thus, the memory is superbly suited to use with multi-user operating systems. The M9900 64K board is designed and factory adjusted to work with the M9900 CPU at either 2 Mhz or 3 Mhz.

2.2.2. Dynabyte 16K Dynamic

The Revision 4B board requires a one-trace modification to pull the memory read signal from the status bus rather than the data bus. We understand from Dynabyte that this modification has been made on their boards revision 4F and later, but have not yet tried

such a board. The modified 4B board works fine, except that it will not run with our Alpha Micro AM-200 disc controller board. This board fails to refresh itself and loses data if the CPU performs too many 16 bit memory cycles in a row. Hence, systems which use the PROM/RAM board or the M9900 64K RAM should not also use the Dynabyte dynamic memory.

2.2.3. Measurement Systems and Controls 64K (DM6400)

Works fine. This is a superbly designed and executed board which provides 64K of storage on a single card using less power and generating less heat than a typical 8K static card. Refresh is completely transparent, so the CPU is never delayed. This board can be configured for most popular 8 bit CPU boards, as well as for the M9900 CPU. One of the unique features of this board is that S-100 bus lines are recieved through RC filter networks driving Schmitt triggers, which makes the board the least sensitive to bus noise we have ever seen. The correct header jumper configuration is:

Header 1: 1-2 3-4 5-6 9-10 12-13 15-16 17-18
Header 2: 1-16 4-9 5-6

2.2.4. Measurement Systems and Controls 64K (DMB6400)

This is a version of the memory discussed above which provides a bank select capability. Each 16K byte bank of the memory is individually software selectable. Note that, however, this memory lacks the flexible deselect feature of the DM6400, and hence the entire last 16K must be disabled to order to deselect the 4K byte block occupied by the PROM/RAM board. As a result, it makes sense only to order the 48K byte version of this board (DMB4800). The jumpering given in the DMB6400 manual for the M9900 CPU is correct.

2.2.5. Micro Resources 66K

Works fine. This is a 64K dynamic RAM board with optional 2K boot PROM. The board has a parity option, but we haven't used it because it requires software to pre-clear the board before use. This board does not work with the AM-200 controller, but has no problems in systems using no DMA devices. We haven't tried the boot PROM feature.

2.2.6. Central Data Corporation 64K

This board is not compatible with the M9900 CPU. It has several options for selecting internal timing and refresh modes, but cannot be jumpered so that it will refresh itself during the intervals available for that purpose on the M9900 CPU.

2.3. PROM Boards

2.3.1. Cromemco Bytesaver

Works fine. Software is supplied with the M9900 CPU to use this board as a PROM programmer.

2.3.2. Ibex 16K PROM Board

Works fine.

3. Peripheral Interfaces

3.1. Serial I/O boards

3.1.1. Marinchip Printer Interface

The Marinchip Printer Interface is a PROM/RAM board with only the Serial I/O section built up. The board is programmed via the CRU interface. Its advantages are fully programmable baud rate, an interrupt mode that really works, and the availability of the real time clock section for user application. It can be ordered set up so that the Texas Instruments 810 printer can be just plugged in and will run at full speed without special cables, option jumpers, or other nonsense. Its disadvantages are the fact that you get only one port per board, the fact that it cannot be used with CPUs other than the 9900, and its fairly high per-port cost.

3.1.2. SSM IO-4

The SSM (formerly Solid State Music) IO-4 board provides two serial and two parallel ports on one board. This board is easy to assemble and configure, very flexible, and about the lowest price per port we've seen. The baud rate, UART modes, and status bits are set up via DIP switches and jumpers, so you can forget software mode setting unless you want to modify the board extensively. Interrupt support is crude.

3.1.3. Godbout Interfacer

Works fine. This is a two port serial I/O board. There is currently a design flaw in the interrupt logic on this board. If you intend to use it in interrupt mode, please contact us for the fix.

3.1.4. IMSAI SIO2-1 and SIO2-2

Works fine. When using this device to interface the system console, the SIO2 board address should be jumpered to zero (IMSAI standard). This board is no longer manufactured.

3.1.5. Processor Technology 3P+S

Works fine, but must be modified due to a design problem in the interrupt logic in the 3P+S. The interrupt logic in the 3P+S uses six open-collector inverters to drive the vectored interrupt lines. If the inputs to these inverters are left unconnected, they generate a constant LOW signal on the vectored interrupt line, and consequently cause a continuous interrupt which causes the processor to hang. In many 8080 and Z-80 systems, where interrupts are never enabled, this causes no problem. In the 9900, interrupt 0 is non-maskable, so the processor will hang in an interrupt loop. To correct this problem, remove IC19 and IC30, which are the drivers for the Vectored Interrupt bus. IC30, however, is also used to drive the output strobes on the parallel ports, so if you require an output strobe you must cut pins 10 and 12 off IC30 to disconnect it from the interrupt bus. When using the 3P+S to interface the system console device, it should be strapped so that the data I/O port is 21 (hex), and the status port is 20 hex. Bit 7 (hex 80) in the status port should be jumpered to Transmitter Buffer Empty, and bit 6 (hex 40) should be

jumpered to Receive Data Available. This board is no longer manufactured.

3.2. Parallel I/O boards

3.2.1. SSM IO-4

The SSM (formerly Solid State Music) IO-4 board provides two serial and two parallel ports on one board. The parallel ports use the Intel 8212 chip, and each 8 bit port may be used bidirectionally.

3.2.2. IMSAI PIO6-3 and PIO 6-6

Works fine. This is a marvelous, fully-programmable parallel I/O board using the Intel 8255 chip. This board is no longer manufactured.

3.2.3. Processor Technology 3P+S

See comments under Serial I/O above. This board is no longer manufactured.

3.3. Video Interface Boards

3.3.1. Alphanumeric Displays

3.3.1.1. Dynabyte Naked Terminal Model 57

Works fine. This is a very unique device. It plugs into the mainframe and attaches to a video monitor and keyboard, and emulates a terminal and serial I/O board. Since it looks like a serial terminal to the CPU, instead of like a memory, it may be

used with the M9900 CPU with no software modifications. Order the M9900 software generated for the Processor Technology 3P+S. Set the DIP switches on the Naked Terminal as follows:

```
Data port:  21
Data ready: 40 S1+ closed, S1- open
Busy:       80 S2+ open, S2- closed
Options:    S31-S33 open, S34 closed
            S35 closed, others up to you
```

You can also make the Naked Terminal emulate the IMSAI SIO2, so you can use software generated for that device. The options should be set the same as for the 3P+S, but the port and ready bits should be set as follows:

```
Data port:  02
Data ready: 02 S1+ closed, S1- open
Busy:       01 S2+ open, S2- closed
```

3.3.1.2. SD Systems VDB

This board is identical in concept to the Dynabyte Naked Terminal discussed above, but is a substantially "smarter" terminal. It lacks the configuration switches of the Naked Terminal, however, so if you intend to use it with the M9900 CPU, you must obtain a special boot ROM and system disc from us which are configured for the VDB. The board works fine.

3.3.1.3. Processor Technology VDM-1

Works fine. At present, however, Marinchip software does not support the VDM-1 as the system terminal device. You can, however, use it for your own display applications. This board is no longer manufactured.

3.3.2. Graphic Displays

3.3.2.1. Digital Video Systems CAT-100

Works fine. The capabilities of this board just go on and on. It can display simple bit graphics with a resolution of 512 by 512

bits, or resolution can be traded for gray scale or for color. The unit (it's a two board set) can also capture a video signal in real time, digitise it, and store it in its internal memory for processing by the computer. The input has all the variable resolution features as the output. A light pen may be attached, and the CAT-100 will return the coordinates where the light pen is seen. A camera shutter sync feature lets you take perfect pictures of the output. Oh yes, it also has an alphanumeric mode where you can store 32K characters and scroll them on a raster line basis (smooth scroll). If this isn't enough, you can add expansion memory to increase the resolution. The CAT-100 includes the image memory, which is accessed through a 2K or 8K byte "window". Thus, increasing the video memory does not decrease the address space left for programs in the system.

3.3.2.2. Vector Graphic High Resolution Graphics

Works fine. This is a raster graphics board from Vector Graphics. Its basic resolution is 256 by 256, but you can trade resolution for gray scale. It requires a Vector Graphics 8K RAM board as its refresh memory.

3.4. Analog Interface Boards

3.4.1. Cromemco D+7AIO

We have never tried or even seen one of these boards, but we understand that it uses the status signals from the data bus, so it will not run without modification.

3.4.2. Vector Graphics Precision Analog Interface

Works fine.

3.5. Real Time Clock Boards

3.5.1. IMSAI PIC-8

The IMSAI PIC-8 board was designed as a combination interrupt controller and real time clock for the IMSAI 8080. By performing fairly major surgery on this board it can be turned into a usable interrupt clock for the M9900 system. We do not recommend that anybody go out and buy a PIC-8 and then hack it up, but if you own one, here is something you can do with it. Assuming you have a fully assembled board, remove the 8214 chip at position E2 and the 8T98 chip at position E6. Then, carefully remove the eight pull-up resistors on the vectored interrupt bus, R9 through R16. Cut the trace from B4 pin 9 to A4 pin 4, and install a jumper wire from A5 pin 15 to A4 pin 4. What you have just done is to totally remove the priority interrupt service logic from the PIC-8 (which would conflict with the logic on the M9900 CPU itself), and modify the way in which the real time clock is reset. The address strapping and clock interrupt strapping remains as documented in the IMSAI manual. To program the modified board, use bits 4 through 6 in the output data to select the interrupt interval per IMSAI documentation. Bit 7, which IMSAI did not use, becomes the clear signal for the clock interrupt request. To enable the clock, output bit 7 and one of the rate select bits. The interrupt service routine must output a byte with bit 7 zero to reset the interrupt request, then resend the rate with bit 7 set. This board is no longer manufactured.

3.6. Tape Interface Boards

3.6.1. Processor Technology CUTS

Works fine. In our opinion this is the most reliable and easy to use audio cassette interface around. It reads and writes either "Kansas City" standard 300 BPS tapes, or CUTS format 1200 BPS tapes. Marinchip Systems does not currently provide software that uses the CUTS interface, but user programs can use the CUTS board to read and write tapes. This board is no longer manufactured.

3.7. Disc Controllers

3.7.1. Tarbell Floppy Disc Interface model 1011

Works fine, but requires the Marinchip PROM/RAM board. This is a non-DMA controller, and requires the 16-bit memory on the Marinchip PROM/RAM board to operate. A Boot PROM is available to load the operating system from this controller. Note: it is not possible to reformat discs when using this controller. Since discs are already formatted when received, this is not usually a problem. This controller is a very simple and straightforward design that is extremely versatile in interfacing to various drives. It comes with information on how to strap it to run most of the popular drives on the market (including PerSci). While the 16-bit PROM/RAM board is required, the low price of the Tarbell controller still results in a large savings going this way. Remember, however, that with a non-DMA controller, the processor is locked up during disc transfers, which may be a problem if you intend to do real-time or multitasking applications.

3.7.2. Telétek FDC-II

This is a buffered controller which supports either single or double density operation. The controller operates by transferring data to and from the disc into a 1K byte buffer RAM which also appears in the CPU address space. Thus, data transfer occurs concurrent with CPU operation, as with a DMA controller, but there are no memory compatibility problems, as with many DMA controllers. Marinchip Systems can provide boot ROMs for the PROM/RAM board which load the operating system from this controller, as well as versions of Marinchip software adapted for this controller. If this controller is purchased from Marinchip Systems, it will be already jumpered for operation with the M9900 CPU. If you purchase it elsewhere, contact us for the correct jumpering to ensure correct operation. The board does not come with interrupts as a standard feature, but Marinchip has developed an engineering change to the board which implements them. Contact us for the two wire change which implements interrupts on the FDC-II if you plan to use interrupts, or use the FDC-II with NOS/MT.

3.7.3. Alpha Microsystems AM-200 FDC

Works fine. The controller can be used with both the PerSci drive, and with conventional floppies (such as the Wangco). The controller must be re-strapped for standard S-100 operation, and if a revision A controller, several fixes must be made on the

board (no fixes are required for revision B and later models). Request "Tech Tip 2" from Alpha for information on S-100 strapping and the fixes for old boards. The 1K PROM on the board is used for the M9900 disc boot: PROMs for this application are available from Marinchip Systems.

3.7.4. Konan SMC-100 Hard Disc Controller

This is a controller for hard disc systems which conform to the "storage module" interface standard. The controller can operate in either DMA or buffered mode (our software supports both), and can control up to 2400 megabytes of disc per controller. This controller is supported by the Network Operating System (both single user and multi user versions), which can be configured for the various drives supported by this controller.

4. Mainframes

The M9900 CPU is very undemanding on a mainframe (chassis and power supply). It uses about 1.5 amps of +8 and small amounts of +16 and -16 current. Its signals have long settling times, and it uses very good line driver and receiver circuits, so it is very tolerant of noisy bus lines. In general, other boards will encounter problems caused by the mainframe before the M9900 CPU does. But why ask for trouble? We recommend a sturdy mainframe with adequate power and an actively terminated mother board. A list of mainframes and mainframe-related components which have been tested with the M9900 CPU are listed below.

4.1. TEI MCS-112

Works fine. This is the 12 slot mainframe from TEI. It comes with a ferroresonant constant-voltage power supply, 12 slot motherboard, and (we understand) now includes termination for all data lines. All power lines to the mother board are fused (other vendors, please take note), and all lines connected to the power mains are shielded from stray fingers.

4.2. Parasitic Engineering Equibox

Works fine. This is the Equinox 100 without the front panel. This system has 20 slots on the magnificent Morrow shielded and

terminated motherboard, and the Parasitic constant-voltage power supply.

4.3. Integrand

Integrand makes a wide selection of mainframes, all of which work fine with the M9900 CPU. Especially nice is a box which contains a 10 slot motherboard and also holds two Shugart or Siemens 8 inch disc drives. The mainframe supplies power for both the discs and the S-100 boards.

4.4. IMSAI 8080

Works fine. Use the Godbout active terminator (see below) if you want to clean up the noisy bus. Note: the front panel lights will properly display the operation of the M9900 CPU, but the only switches that work are POWER, RESET, EXTERNAL CLEAR, RUN, STOP, and SINGLE STEP.

4.5. Vector 1

Works fine. Very solid mechanical construction.

4.6. Godbout active terminator

Works fine. This is a board which retrofits active termination to a motherboard that doesn't have termination. Note that active termination (as provided by this board) draws much less power from the power supply than passive resistor termination, yet is just as effective in reducing noise.